

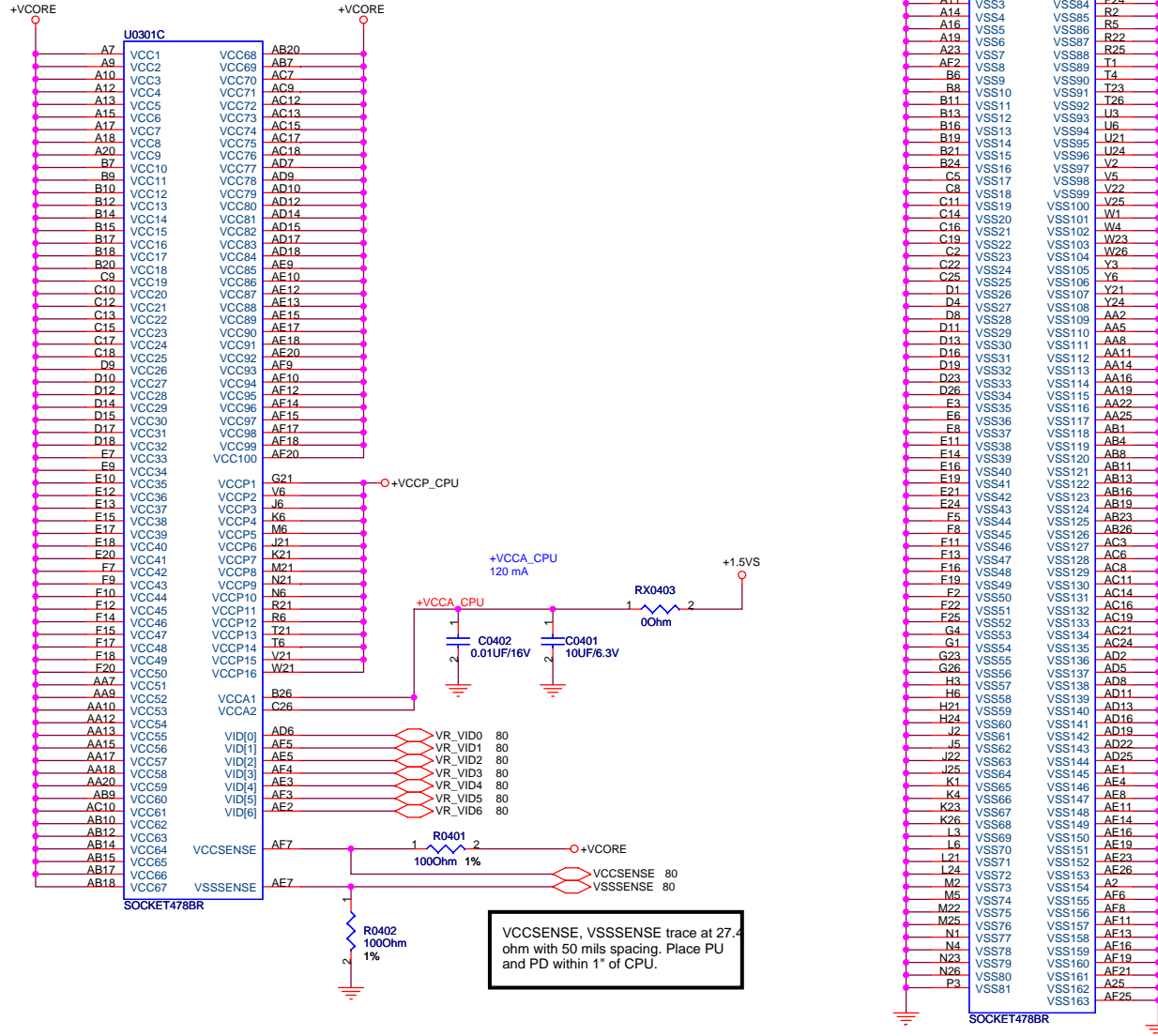


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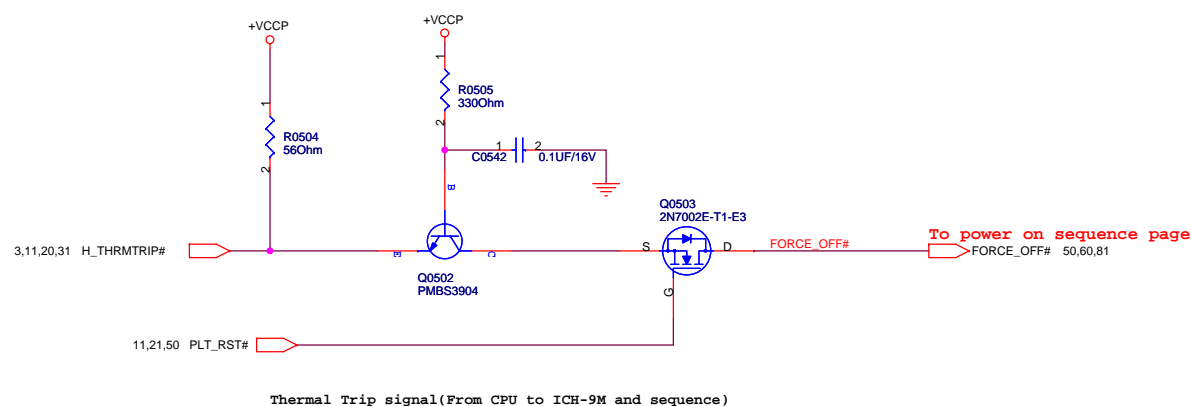
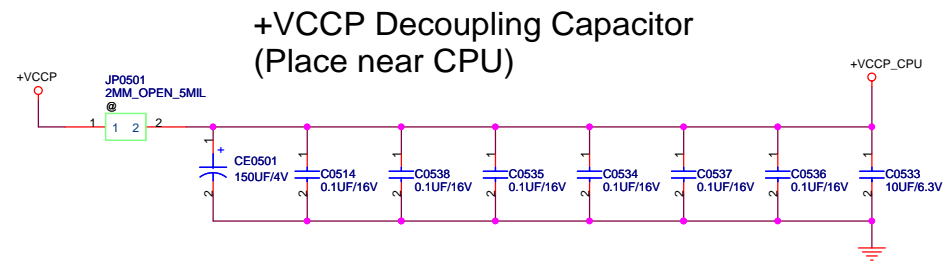
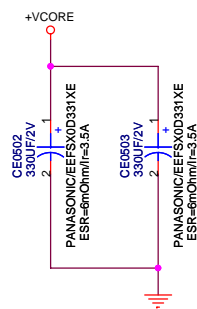
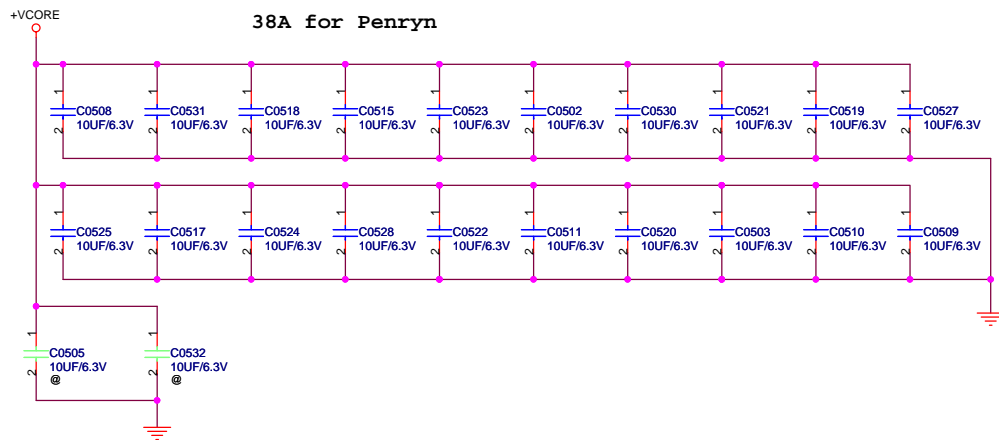
WWW.AliSaler.Com

GPIO 60	Native	RTLAN_DSM_EN	+3VSUS
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


Size Custom	Project Name Rocky30	
Date: Tuesday, January 15, 2008	Sheet 2 of 94	



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



5		4		3		2		1	

+3VS  +3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92
 +1.8V  +1.8V 8,9,11,13,83,91
 M_VREF_MCH  M_VREF_MCH 8,9,11

SMBus Slave Address:A0H

temp_5886_t101
 (12G025M22000LV with 12G025C2200WLV
 co-lay symbol)

SMBus Slave Address: A0H

Place near SO-DIMM_0

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these caps near SO DIMM 0

VREF -> 10/10 mils

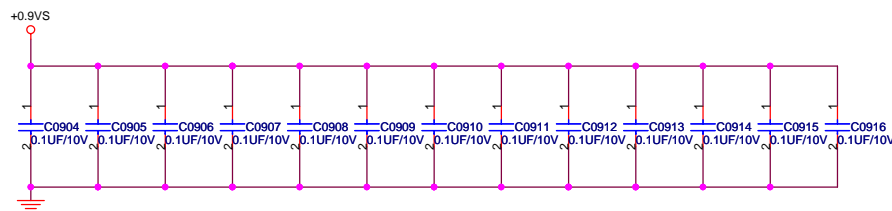
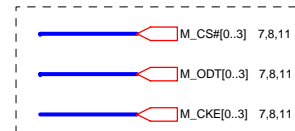
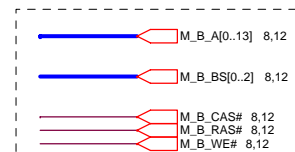
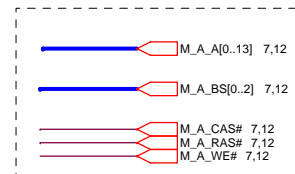
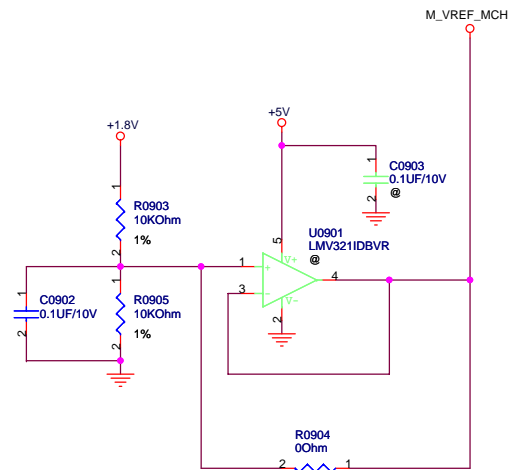
SO-DIMM 0 is placed nearer the
 GMCH than SO-DIMM 1

Layout Note: Place these Caps near SO DIMM 0

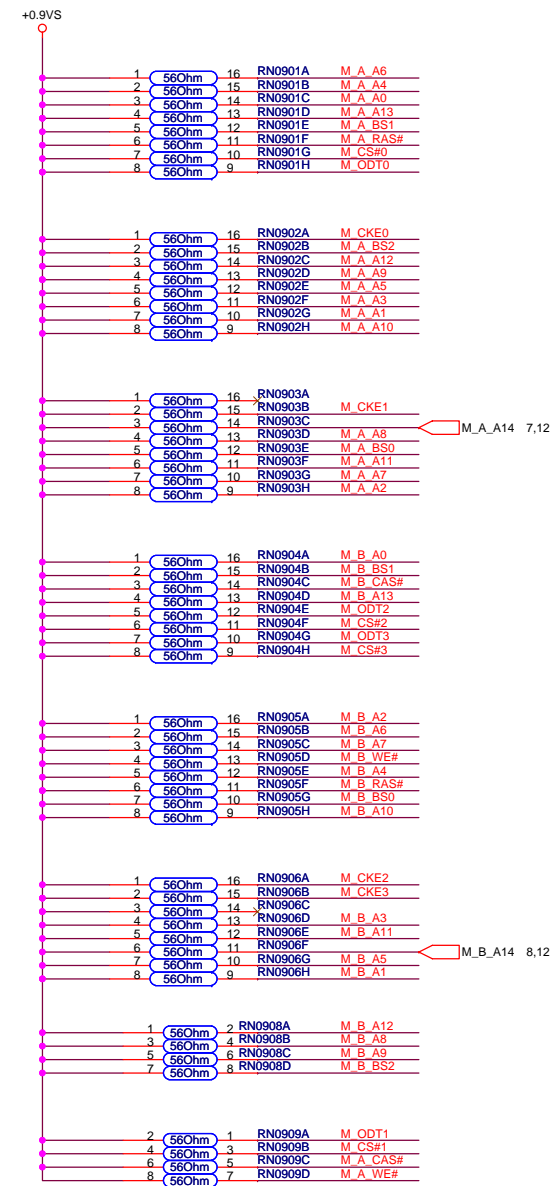
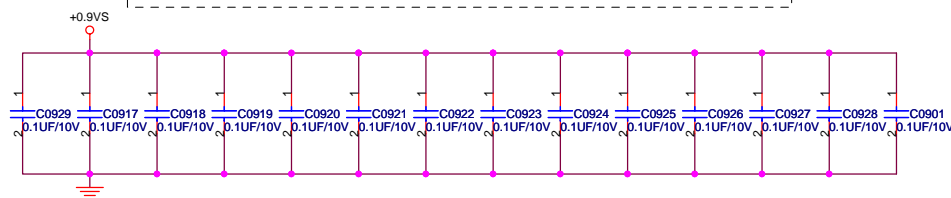
PLACE NEAR SO-DIMM_0 / SO-DIMM_1

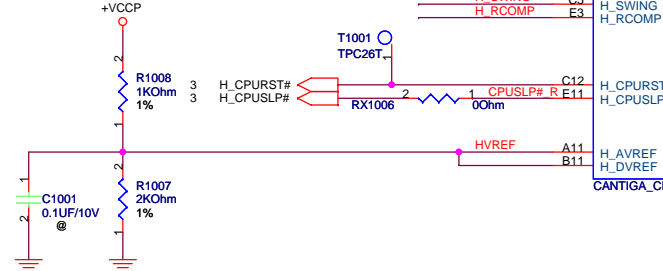
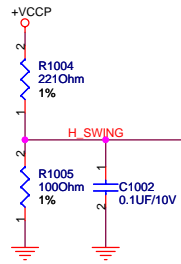
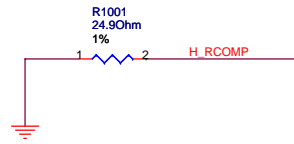


+5V +5V 44,56,57,91
 +1.8V +1.8V 7,8,11,13,83,91
 M_VREF_MCH M_VREF_MCH 7,8,11
 +0.9VS +0.9VS 83

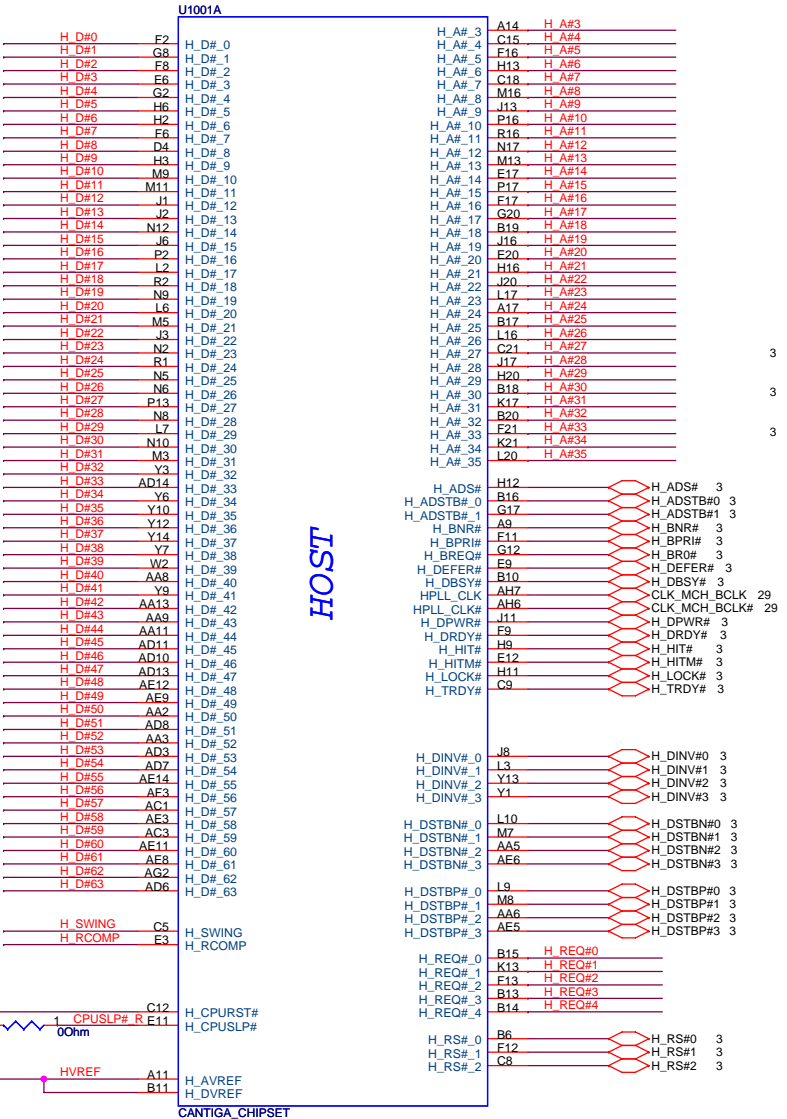


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





CAP 0.1u within 100 mils from GMCH





7 M_A_DQ[0:63]

M A DQ0 AJ38
 M A DQ1 AJ41
 M A DQ2 AN38
 M A DQ3 AM38
 M A DQ4 AJ36
 M A DQ5 AJ40
 M A DQ6 AM44
 M A DQ7 AM42
 M A DQ8 AN43
 M A DQ9 AN44
 M A DQ10 AU40
 M A DQ11 AT38
 M A DQ12 AN41
 M A DQ13 AN39
 M A DQ14 AU44
 M A DQ15 AU42
 M A DQ16 AV39
 M A DQ17 AY44
 M A DQ18 BA40
 M A DQ19 BD43
 M A DQ20 AV41
 M A DQ21 AY43
 M A DQ22 BA41
 M A DQ23 BC40
 M A DQ24 AY37
 M A DQ25 BD38
 M A DQ26 AV37
 M A DQ27 AT36
 M A DQ28 AY38
 M A DQ29 BB38
 M A DQ30 AV36
 M A DQ31 AW36
 M A DQ32 BD13
 M A DQ33 AU11
 M A DQ34 BC11
 M A DQ35 BA12
 M A DQ36 AU13
 M A DQ37 AV13
 M A DQ38 BD12
 M A DQ39 BC12
 M A DQ40 BB9
 M A DQ41 BA9
 M A DQ42 AU10
 M A DQ43 AV9
 M A DQ44 BA11
 M A DQ45 BD9
 M A DQ46 AY8
 M A DQ47 BA6
 M A DQ48 AV5
 M A DQ49 AV7
 M A DQ50 AT9
 M A DQ51 AN8
 M A DQ52 AU5
 M A DQ53 AU6
 M A DQ54 AT5
 M A DQ55 AN10
 M A DQ56 AM11
 M A DQ57 AM5
 M A DQ58 AJ9
 M A DQ59 AJ8
 M A DQ60 AN12
 M A DQ61 AM13
 M A DQ62 AJ11
 M A DQ63 AJ12

U1001D

SA_DQ_0
 SA_DQ_1
 SA_DQ_2
 SA_DQ_3
 SA_DQ_4
 SA_DQ_5
 SA_DQ_6
 SA_DQ_7
 SA_DQ_8
 SA_DQ_9
 SA_DQ_10
 SA_DQ_11
 SA_DQ_12
 SA_DQ_13
 SA_DQ_14
 SA_DQ_15
 SA_DQ_16
 SA_DQ_17
 SA_DQ_18
 SA_DQ_19
 SA_DQ_20
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 SA_DQ_37
 SA_DQ_38
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 SA_DQ_40
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 SA_DQ_44
 SA_DQ_45
 SA_DQ_46
 SA_DQ_47
 SA_DQ_48
 SA_DQ_49
 SA_DQ_50
 SA_DQ_51
 SA_DQ_52
 SA_DQ_53
 SA_DQ_54
 SA_DQ_55
 SA_DQ_56
 SA_DQ_57
 SA_DQ_58
 SA_DQ_59
 SA_DQ_60
 SA_DQ_61
 SA_DQ_62
 SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0
 SA_BS_1
 SA_BS_2
 SA_RAS#
 SA_CAS#
 SA_WE#

SA_DM_0
 SA_DM_1
 SA_DM_2
 SA_DM_3
 SA_DM_4
 SA_DM_5
 SA_DM_6
 SA_DM_7

SA_DQS_0
 SA_DQS_1
 SA_DQS_2
 SA_DQS_3
 SA_DQS_4
 SA_DQS_5
 SA_DQS_6
 SA_DQS_7

SA_MA_0
 SA_MA_1
 SA_MA_2
 SA_MA_3
 SA_MA_4
 SA_MA_5
 SA_MA_6
 SA_MA_7
 SA_MA_8
 SA_MA_9
 SA_MA_10
 SA_MA_11
 SA_MA_12
 SA_MA_13
 SA_MA_14

BD21 M A BS0 7,9
 BG18 M A BS1 7,9
 AT25 M A BS2 7,9
 BB20 M A RAS# 7,9
 BD20 M A CAS# 7,9
 AY20 M A WE# 7,9

AM37 M A DM0
 AT41 M A DM1
 AY41 M A DM2
 AU39 M A DM3
 BB12 M A DM4
 AY6 M A DM5
 AT7 M A DM6
 AJ5 M A DM7

AJ44 M A DQS0
 AT44 M A DQS1
 BA43 M A DQS2
 BC37 M A DQS3
 AW12 M A DQS4
 BC8 M A DQS5
 AU8 M A DQS6
 AM7 M A DQS7

AJ43 M A DQS#0
 AT43 M A DQS#1
 BA44 M A DQS#2
 BD37 M A DQS#3
 AY12 M A DQS#4
 BD8 M A DQS#5
 AU9 M A DQS#6
 AM8 M A DQS#7

BA21 M A A0
 BC24 M A A1
 BG24 M A A2
 BH24 M A A3
 BG25 M A A4
 BA24 M A A5
 BD24 M A A6
 BG27 M A A7
 BE25 M A A8
 AW24 M A A9
 BC21 M A A10
 BG26 M A A11
 BH26 M A A12
 BH17 M A A13
 AY25 M A A14

CANTIGA_CHIPSET

8 M_B_DQ[0:63]

M B DQ0 AK47
 M B DQ1 AH46
 M B DQ2 AP47
 M B DQ3 AP46
 M B DQ4 AJ46
 M B DQ5 AJ48
 M B DQ6 AM48
 M B DQ7 AP48
 M B DQ8 AU47
 M B DQ9 AU46
 M B DQ10 BA48
 M B DQ11 AY48
 M B DQ12 AT47
 M B DQ13 AR47
 M B DQ14 BA47
 M B DQ15 BC47
 M B DQ16 BC46
 M B DQ17 BC44
 M B DQ18 RG43
 M B DQ19 BF43
 M B DQ20 BE45
 M B DQ21 BC41
 M B DQ22 BE40
 M B DQ23 BF41
 M B DQ24 RG38
 M B DQ25 BF38
 M B DQ26 BH35
 M B DQ27 RG35
 M B DQ28 BH40
 M B DQ29 RG39
 M B DQ30 BG34
 M B DQ31 BH34
 M B DQ32 BH14
 M B DQ33 RG12
 M B DQ34 BH11
 M B DQ35 BG8
 M B DQ36 BH12
 M B DQ37 BF11
 M B DQ38 BF8
 M B DQ39 BG7
 M B DQ40 BC5
 M B DQ41 BC6
 M B DQ42 AY3
 M B DQ43 AY1
 M B DQ44 BF6
 M B DQ45 BF5
 M B DQ46 BA1
 M B DQ47 BD3
 M B DQ48 AV2
 M B DQ49 AU3
 M B DQ50 AR3
 M B DQ51 AN2
 M B DQ52 AY2
 M B DQ53 AV1
 M B DQ54 AP3
 M B DQ55 AR1
 M B DQ56 AL1
 M B DQ57 AL2
 M B DQ58 AJ1
 M B DQ59 AH1
 M B DQ60 AM2
 M B DQ61 AM3
 M B DQ62 AH3
 M B DQ63 AJ3

U1001E

SB_DQ_0
 SB_DQ_1
 SB_DQ_2
 SB_DQ_3
 SB_DQ_4
 SB_DQ_5
 SB_DQ_6
 SB_DQ_7
 SB_DQ_8
 SB_DQ_9
 SB_DQ_10
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 SB_DQ_57
 SB_DQ_58
 SB_DQ_59
 SB_DQ_60
 SB_DQ_61
 SB_DQ_62
 SB_DQ_63

SB_BS_0
 SB_BS_1
 SB_BS_2
 SB_RAS#
 SB_CAS#
 SB_WE#

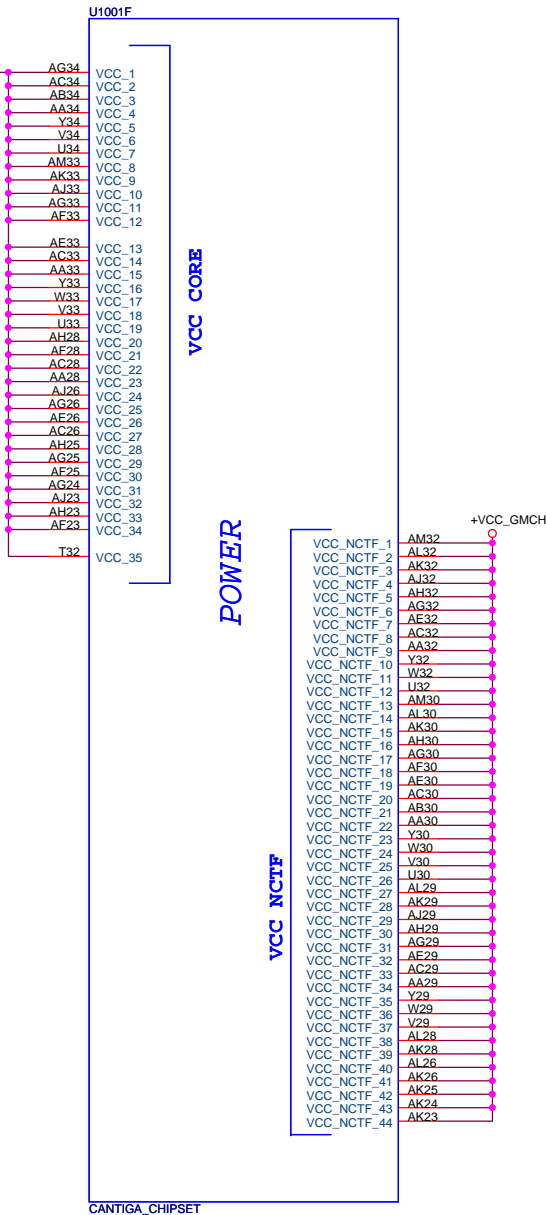
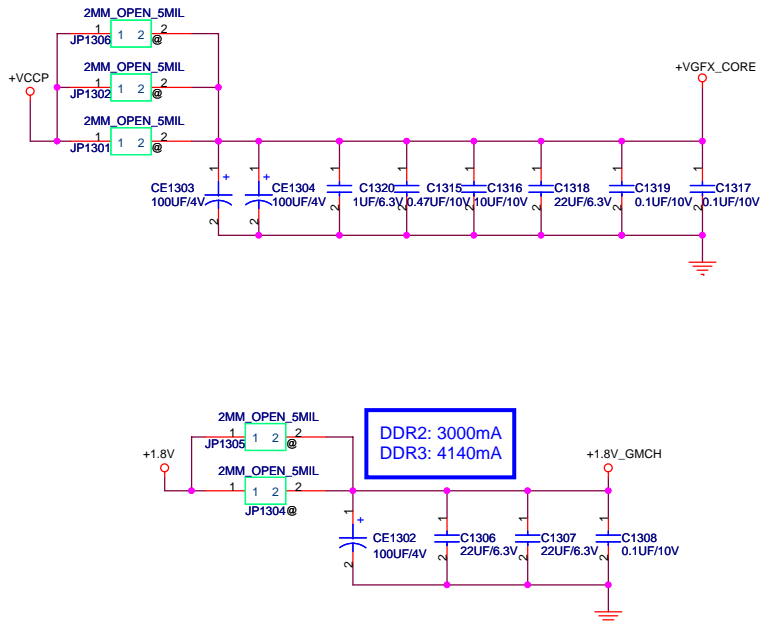
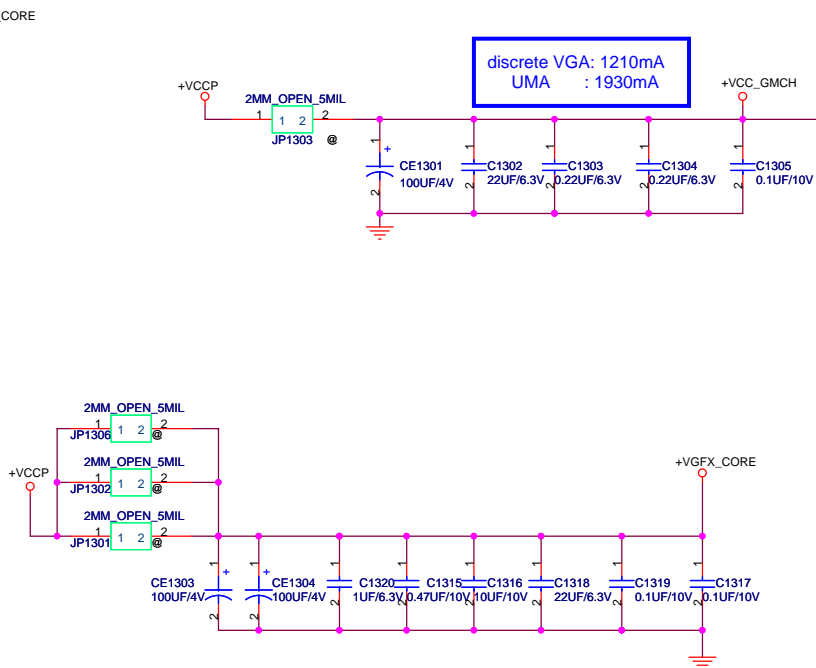
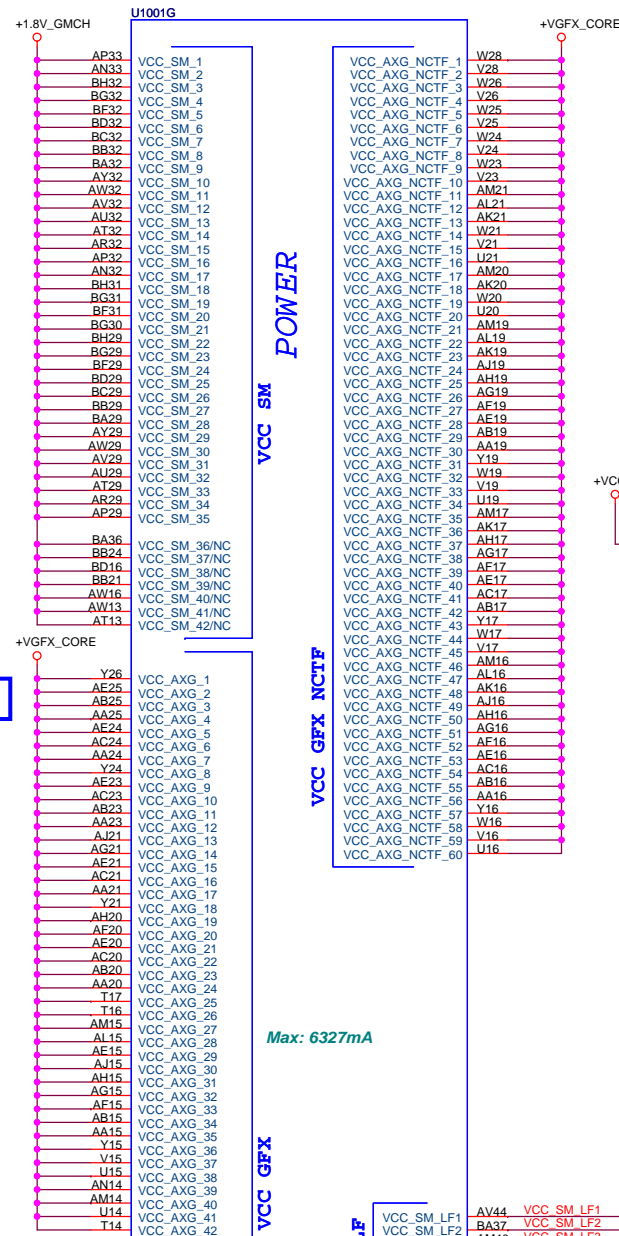
SB_DM_0
 SB_DM_1
 SB_DM_2
 SB_DM_3
 SB_DM_4
 SB_DM_5
 SB_DM_6
 SB_DM_7

AL47 M B DQS0
 AV48 M B DQS1
 BG41 M B DQS2
 RG37 M B DQS3
 BH9 M B DQS4
 BB2 M B DQS5
 AU1 M B DQS6
 AN6 M B DQS7
 AL46 M B DQS#0
 AV47 M B DQS#1
 BH41 M B DQS#2
 BH37 M B DQS#3
 BG9 M B DQS#4
 BC2 M B DQS#5
 AT2 M B DQS#6
 AN5 M B DQS#7

AV17 M B A0
 BA25 M B A1
 BC25 M B A2
 AU25 M B A3
 AW25 M B A4
 BB28 M B A5
 AU28 M B A6
 AW28 M B A7
 AT33 M B A8
 BD33 M B A9
 BB16 M B A10
 AW33 M B A11
 AY33 M B A12
 BH15 M B A13
 AU33 M B A14

CANTIGA_CHIPSET

DDR SYSTEM MEMORY B



T1301 1 AJ14
T1302 1 AH14

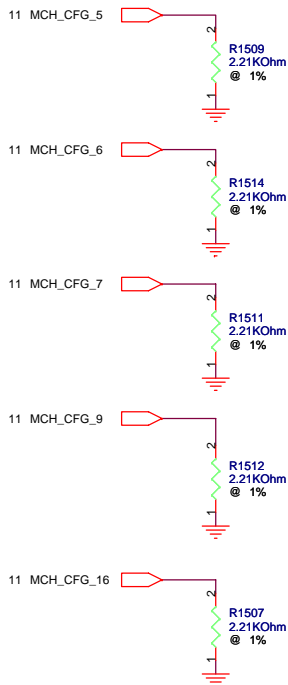
VCC_AGX_SENSE
VSS_AGX_SENSE

Route VCC_AGX_SENSE and
VSS_AGX_SENSE differentially.

Close to GMCH (8 mil trace)

ASUS Title : Cantiga-POWER (4)
Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0
Date: Sunday, January 20, 2008	Sheet	13 of 94



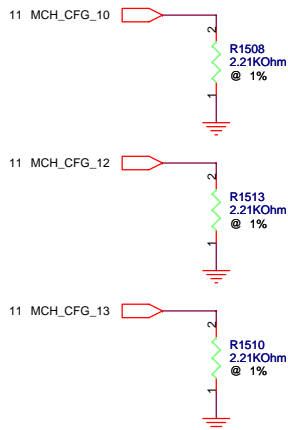
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

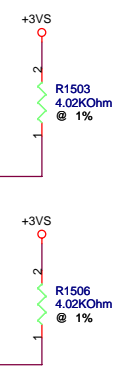
CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable



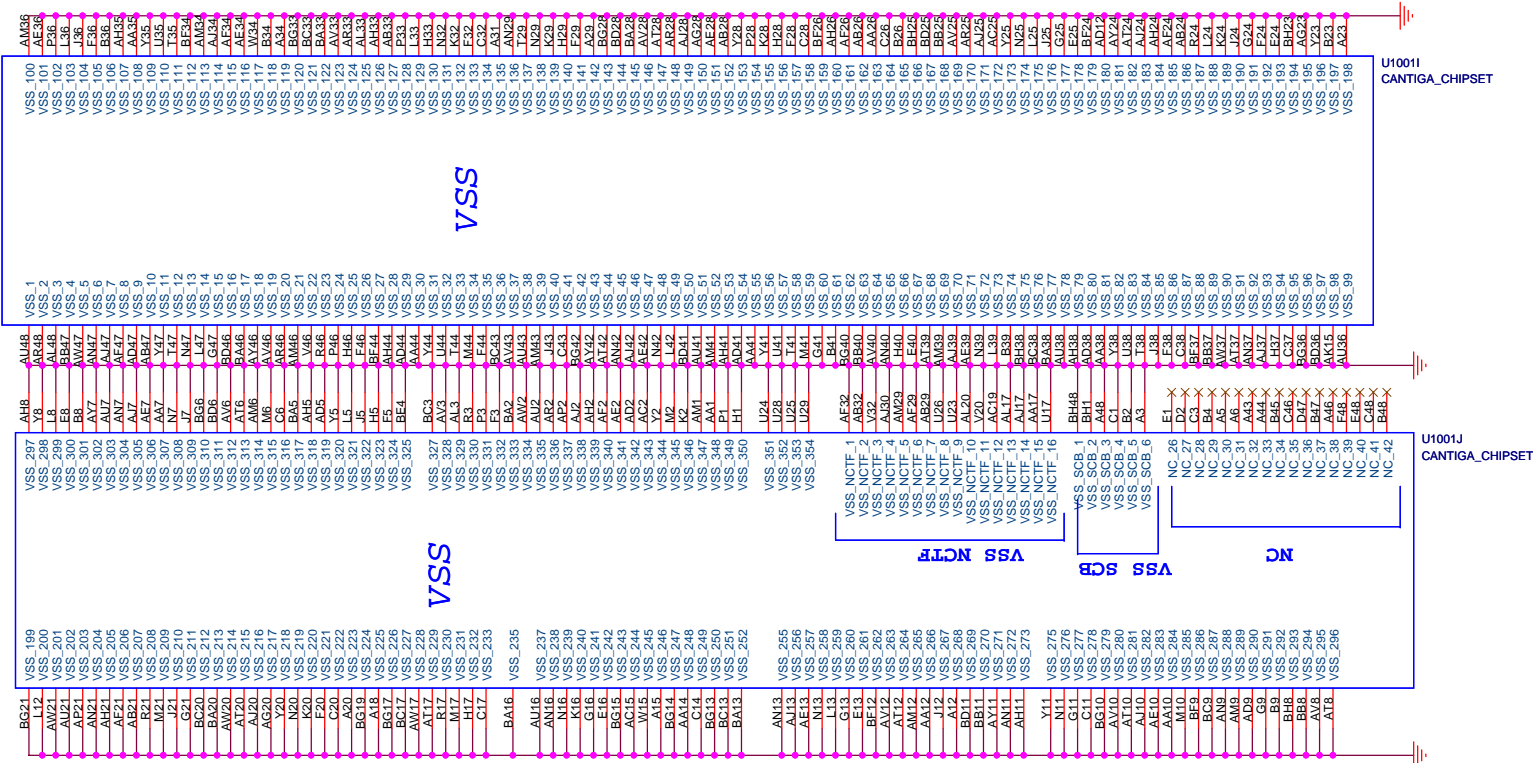
CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)



CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>16</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

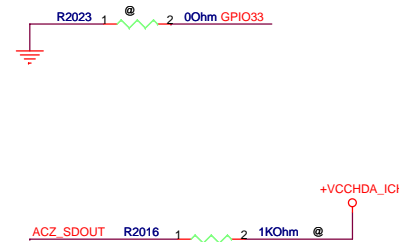
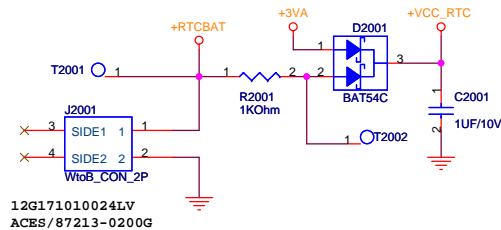
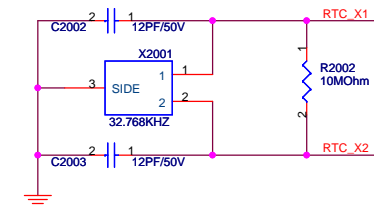
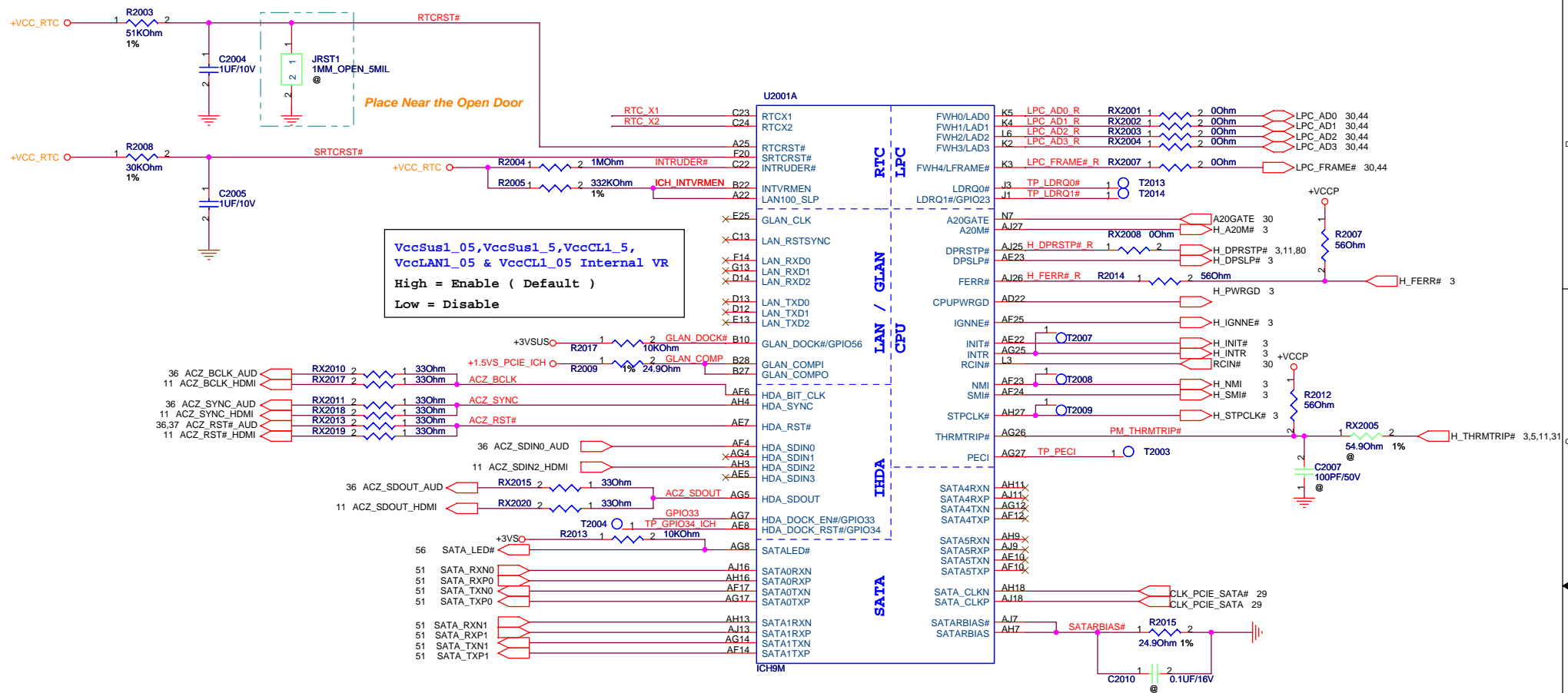
		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>17</i> of <i>94</i>	

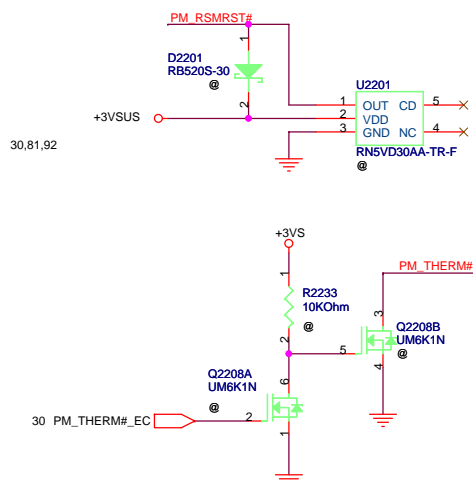
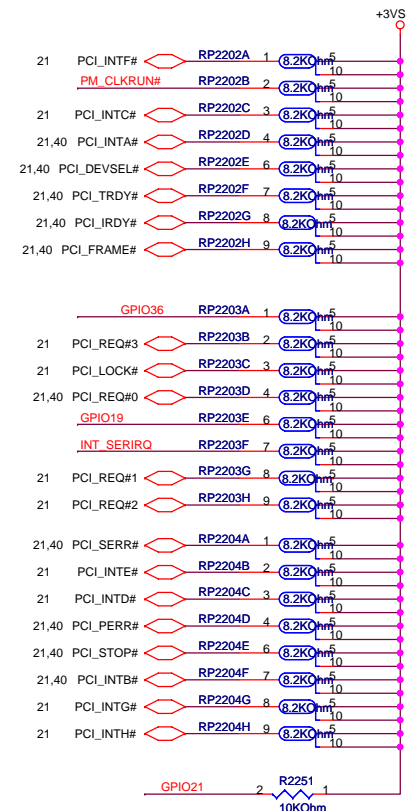
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>18</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>19</i> of <i>94</i>	





	PCB_ID2
14"/15"	L
13"	H

```
CL_VREF0 ~= 0.405 V
```

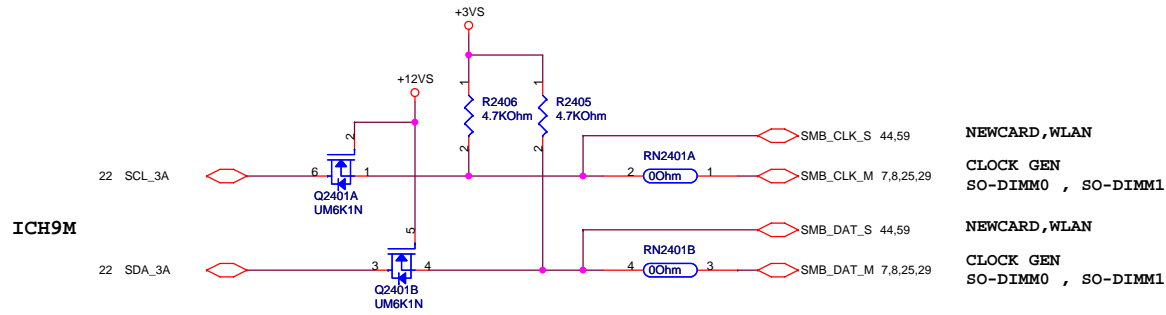
CL_VREF0 routing rules

Width = 12 mils min

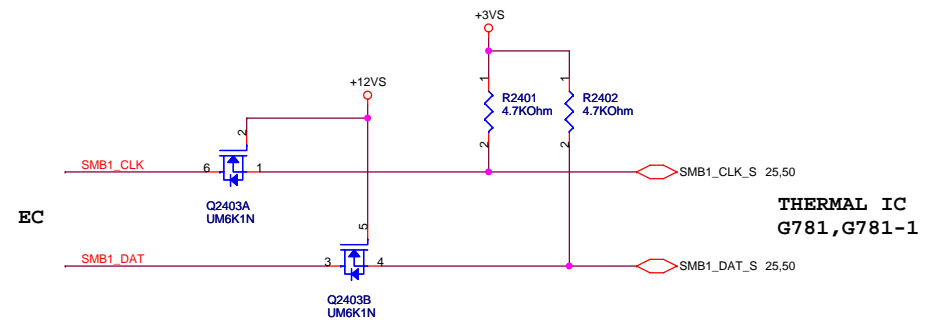
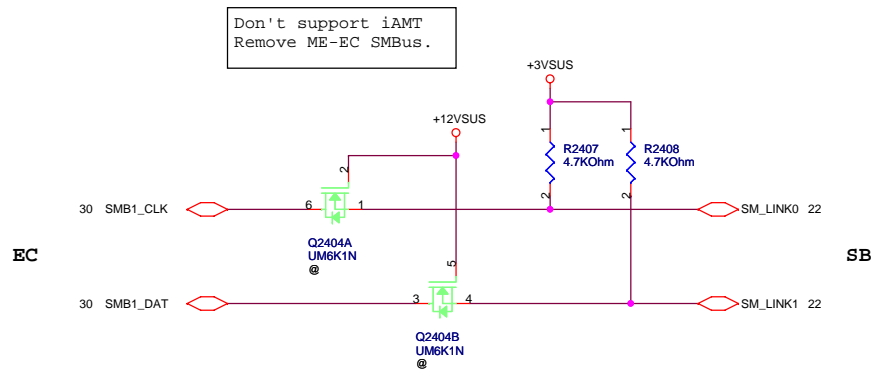
Spacing = 12 mils min

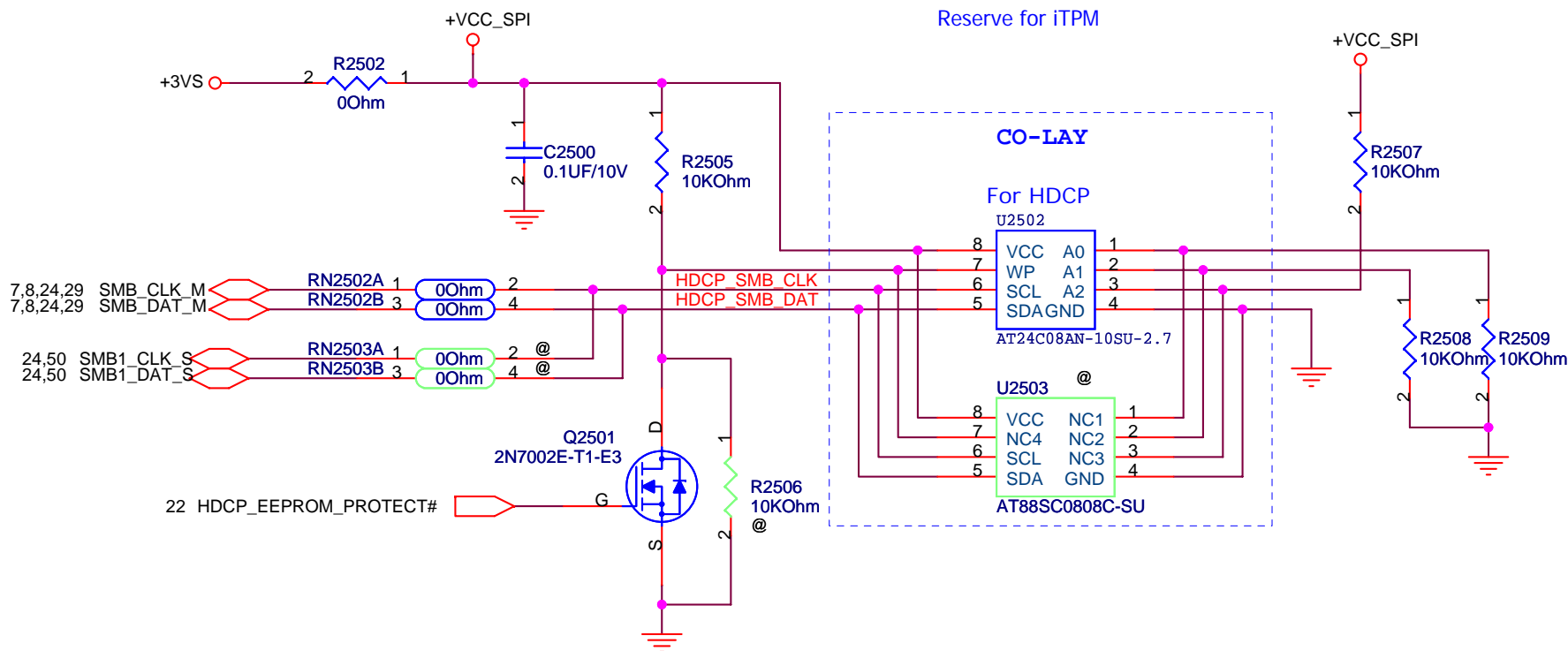
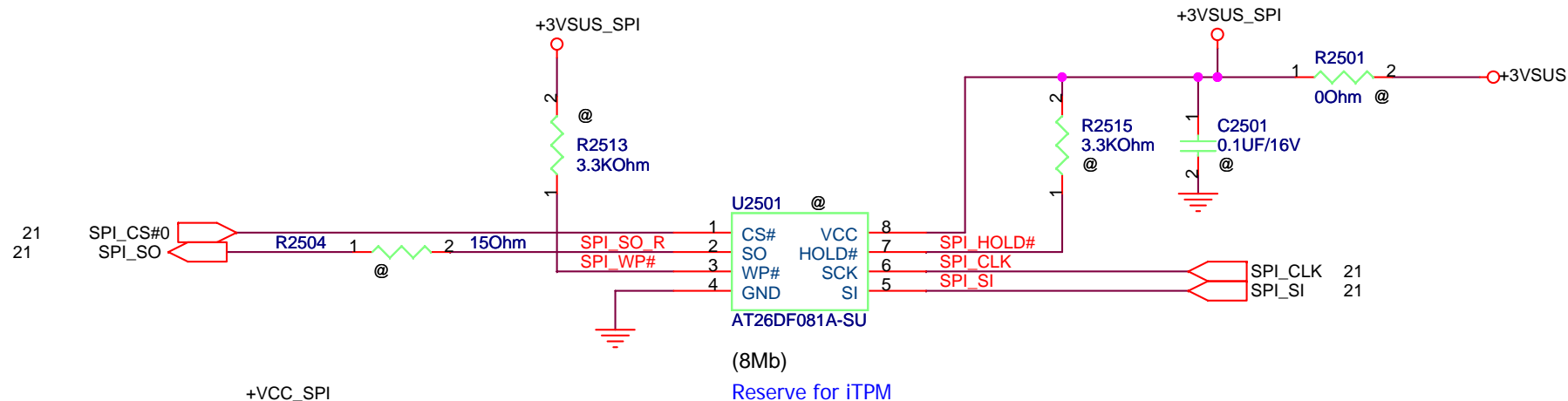
Break-out: 5 mils on 5 mils for 300 mils max

ICH9-M



EC






U2502-AT24C08A :
Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509
Nostuff : R2505

U2503-AT88SC0808C :
Stuff : U2503
Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

ASUS		Title : SPI ROM	
		Engineer: Peter Lo	
Size Custom	Project Name Rocky30		Rev 1.0
Date: Monday, February 04, 2008		Sheet 25 of 94	

	5	4	3	2	1	
D						D
C						C
B						B
A						A
						<div><div></div><div>Title :</div></div>
						Engineer: <i>Peter Lo</i>
Size	Project Name				Rev	
A	Rocky30				1.0	
Date: <i>Thursday, October 18, 2007</i>					Sheet <i>26</i> of <i>94</i>	

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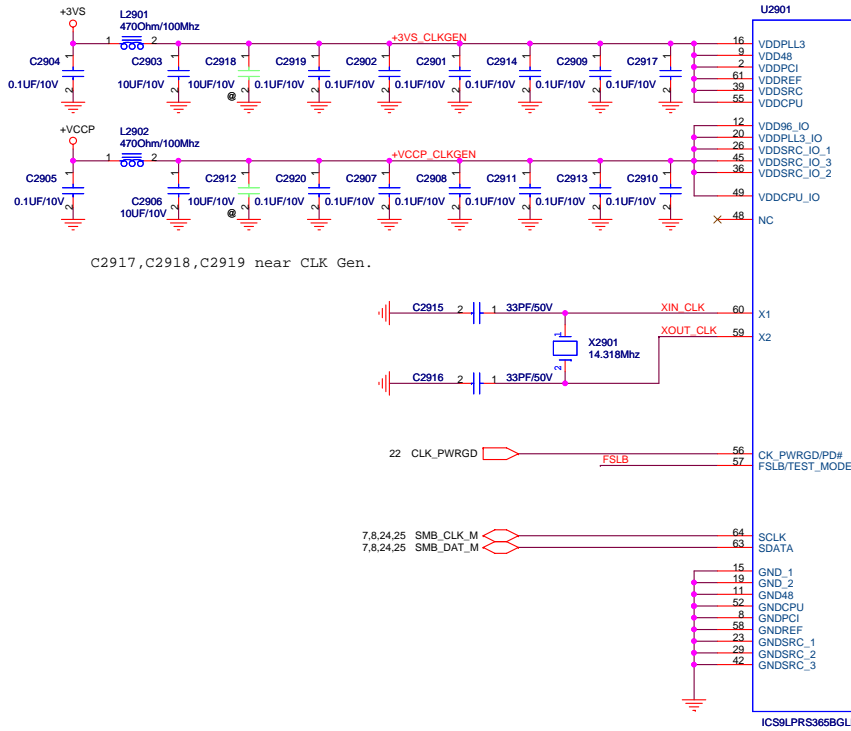
4321

	5	4	3	2	1			
D					D			
C					C			
B					B			
A					A			
<div>ASUS®</div> <div>Title :</div> <div>Engineer: <i>Peter Lo</i></div> <table><tr><td>Size <i>A</i></td><td>Project Name <i>Rocky30</i></td><td>Rev <i>1.0</i></td></tr></table> <div>Date: <i>Thursday, October 18, 2007</i>Sheet <i>27</i> of <i>94</i></div>						Size <i>A</i>	Project Name <i>Rocky30</i>	Rev <i>1.0</i>
Size <i>A</i>	Project Name <i>Rocky30</i>	Rev <i>1.0</i>						

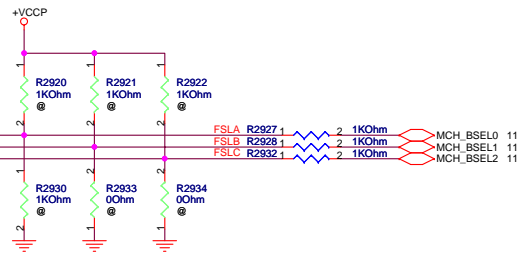
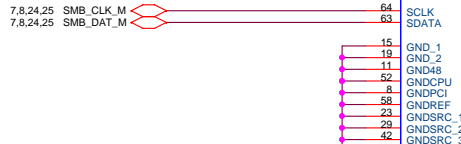
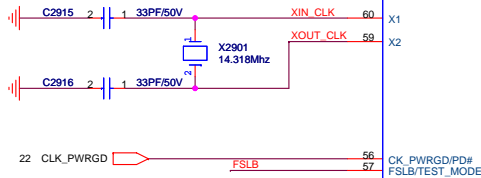
	5	4	3	2	1						
D					D						
C					C						
B					B						
A					A						
					<div>ASUS®</div> <div>Title :</div>						
					Engineer: <i>Peter Lo</i>						
					<table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>A</td><td>Rocky30</td><td>1.0</td></tr></table>	Size	Project Name	Rev	A	Rocky30	1.0
Size	Project Name	Rev									
A	Rocky30	1.0									
					Date: <i>Thursday, October 18, 2007</i> Sheet <i>28</i> of <i>94</i>						

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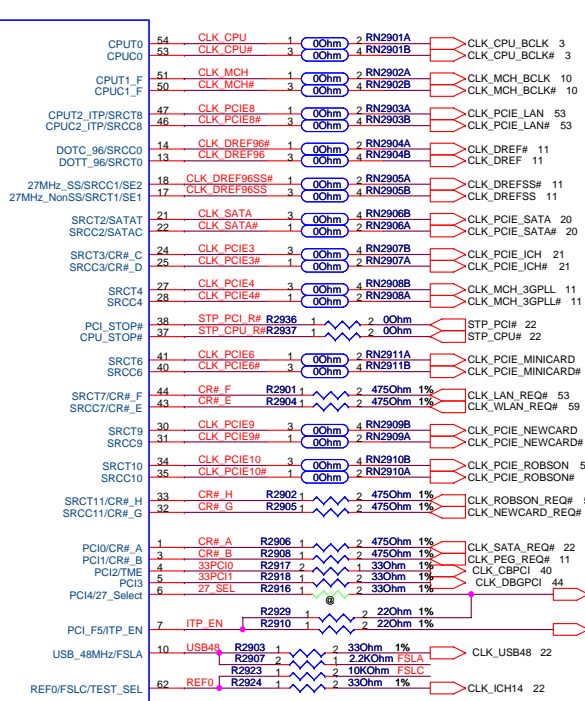
+VCCP 5,10,11,13,14,20,23,80,82
+3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92



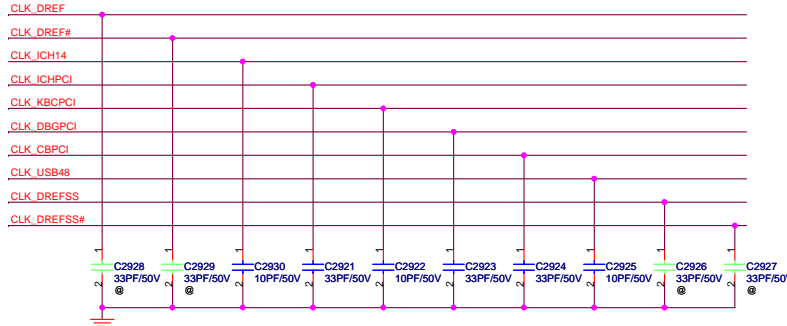
C2917,C2918,C2919 near CLK Gen.



BCLK	FSB	FSLC	FSLB	FSLA
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.



CR#_A	0 = SRC 0	1 = SRC 2	SATA
CR#_B	0 = SRC 1	1 = SRC 4	MCH
CR#_C	0 = SRC 0	1 = SRC 2	
CR#_D	0 = SRC 1	1 = SRC 4	
CR#_E	SRC 6	WLAN	
CR#_F	SRC 8	LAN	
CR#_G	SRC 9	New Card	
CR#_H	SRC 10	Robson	

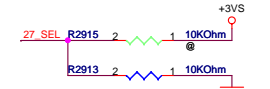
Latched Input Select

0 = SRC 8 Decide pin 46, 47
1 = CPU_ITP CLK



27_Select=0, Decide pin 13/14,17/18
pin#13/14=DOT96;
pin#17/18=LCD_SST;

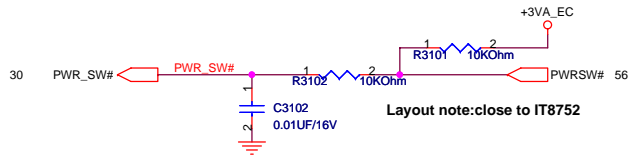
27_Select=1,
pin#13/14=SRC0;
pin#17/18=27MHz non-spread SE clock;



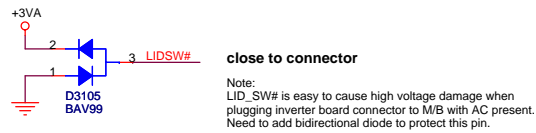
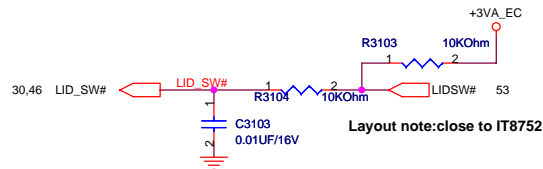
For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.

For Switch

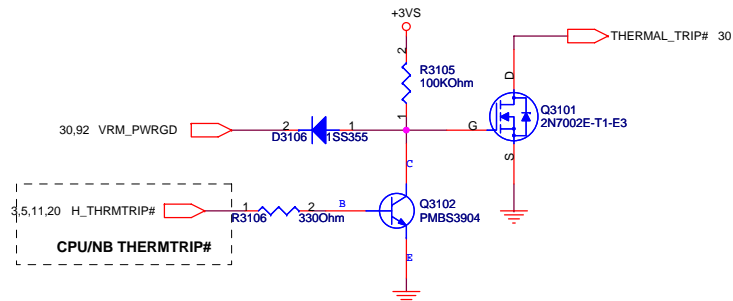
PWR SWITCH



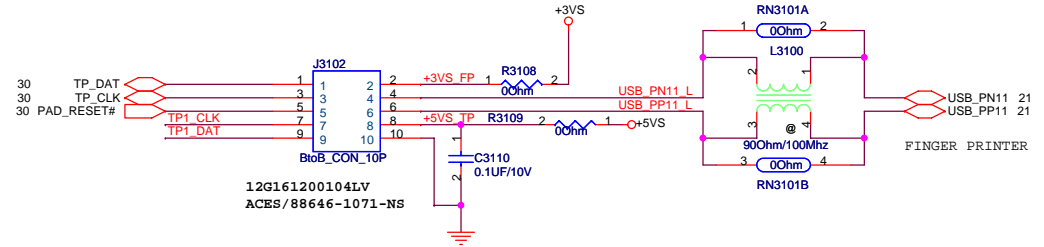
LID SWITCH



For Thermal Control Method

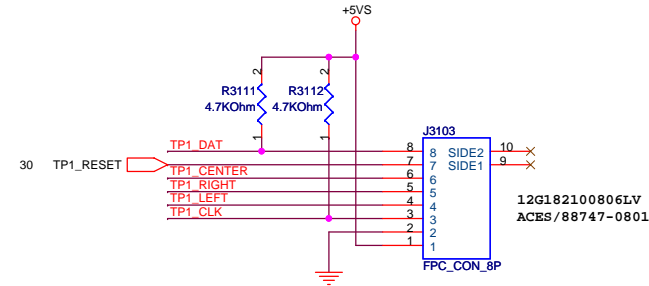


TOUCH PAD CONN

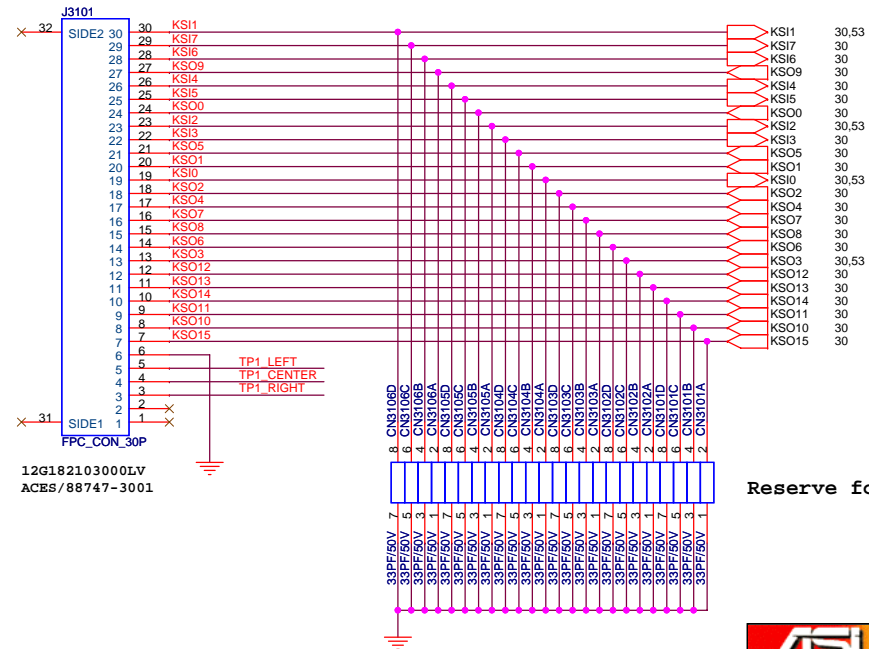


TP : Touch Pad
TP1: Track Point


TRACK POINT CONN



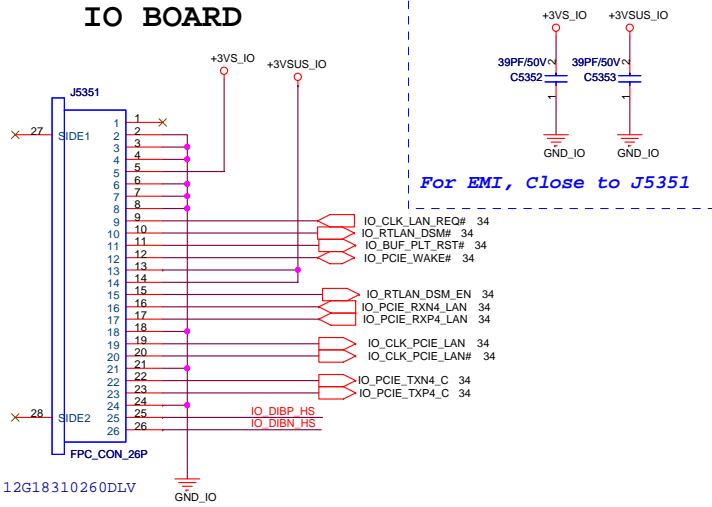
Keyboard Connector



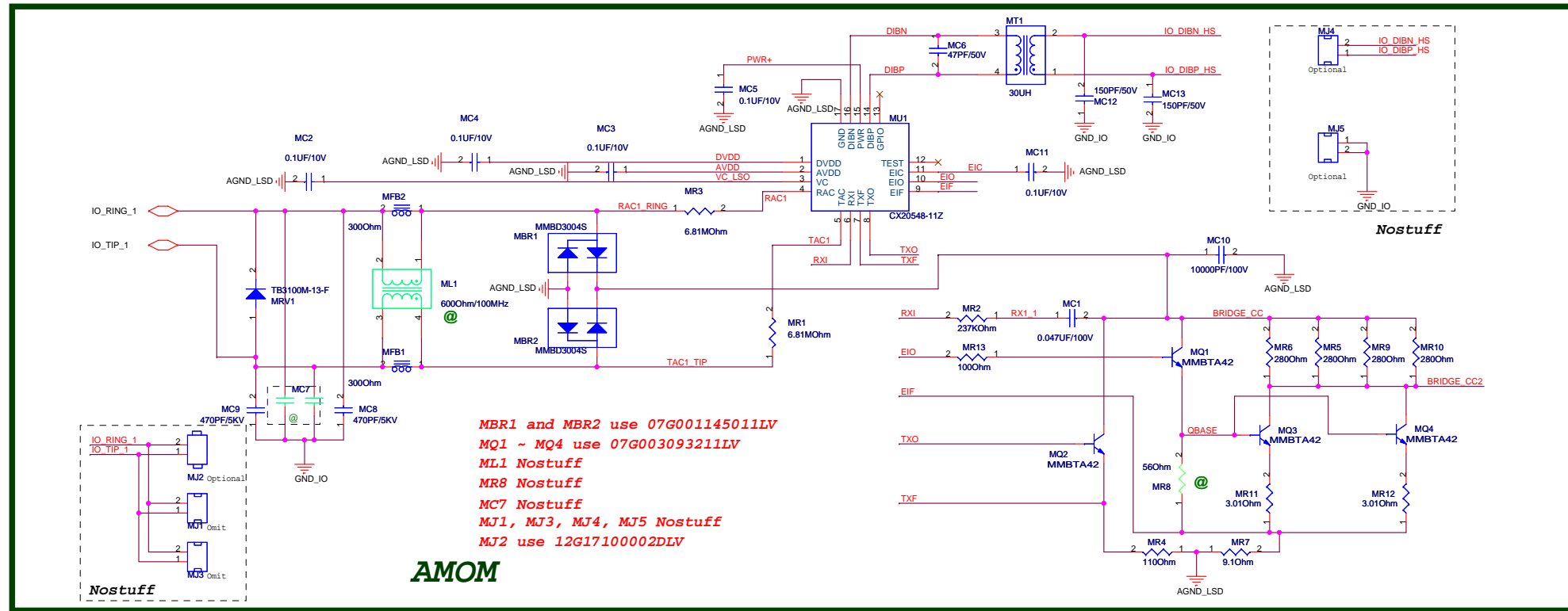


		Title : .	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
Custom	Rocky30		1.0
Date: Sunday, January 20, 2008		Sheet	32 of 94

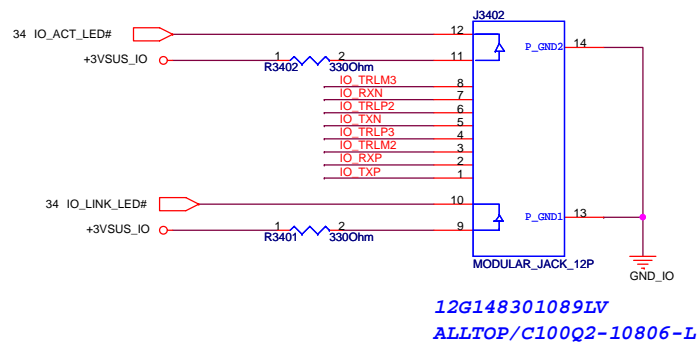
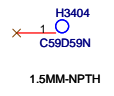
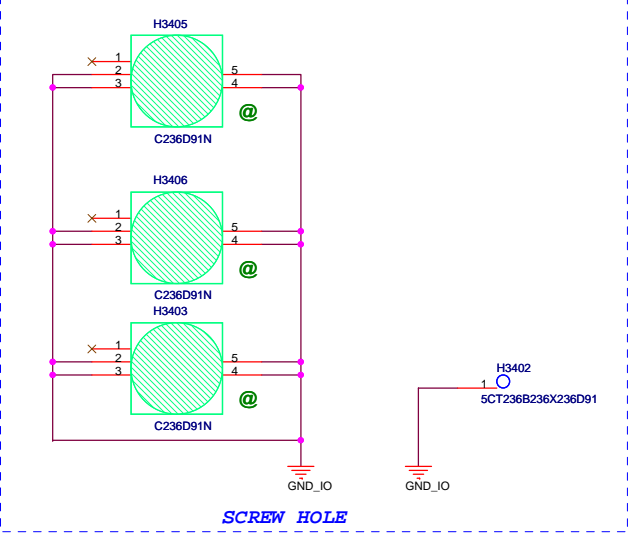
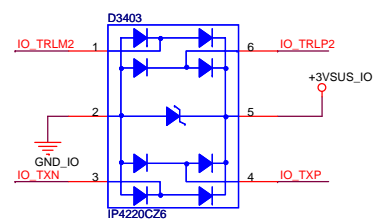
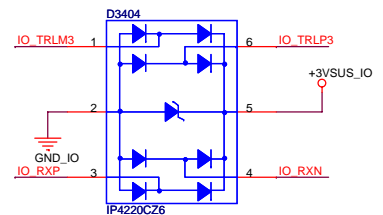
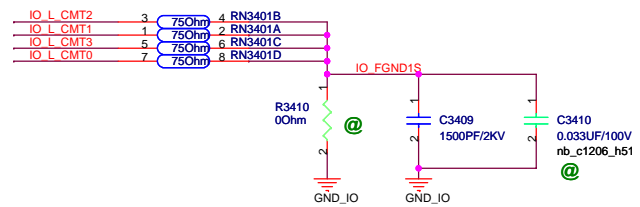
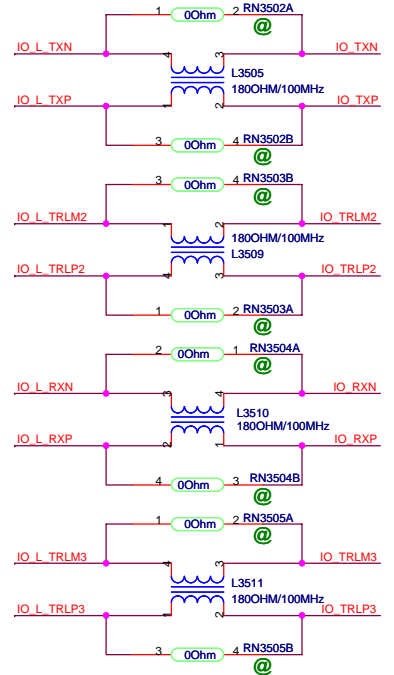
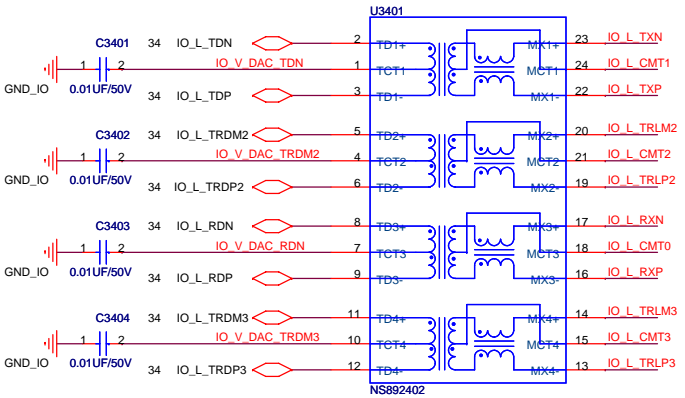
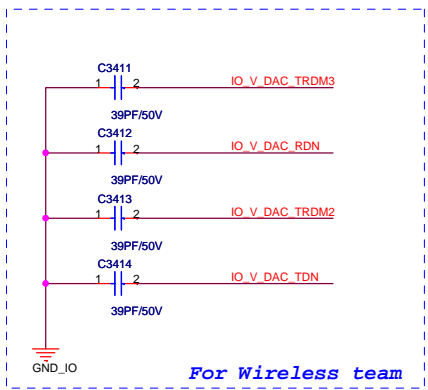
IO BOARD



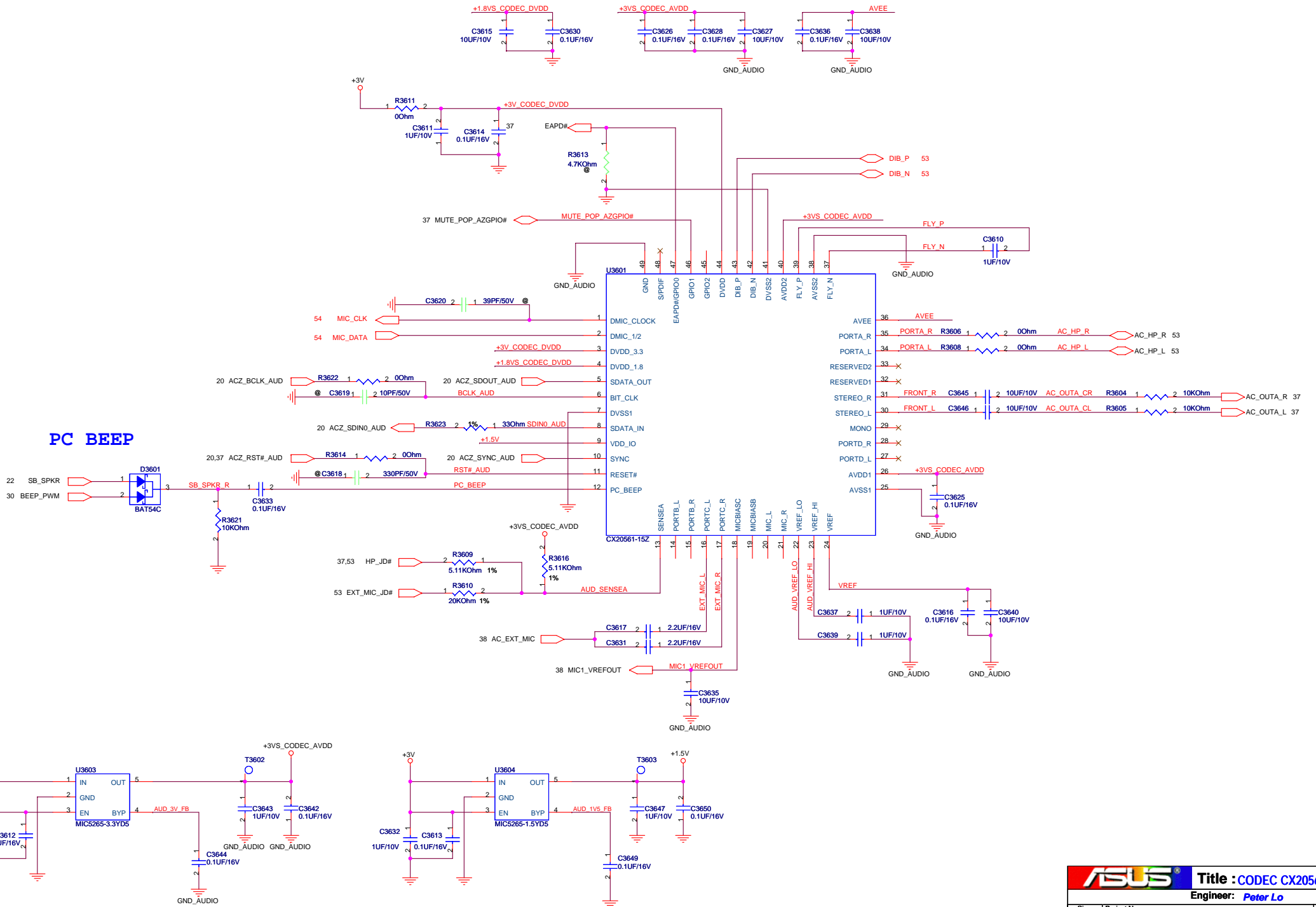
12G18310260DLV



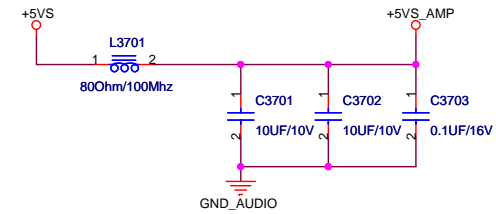
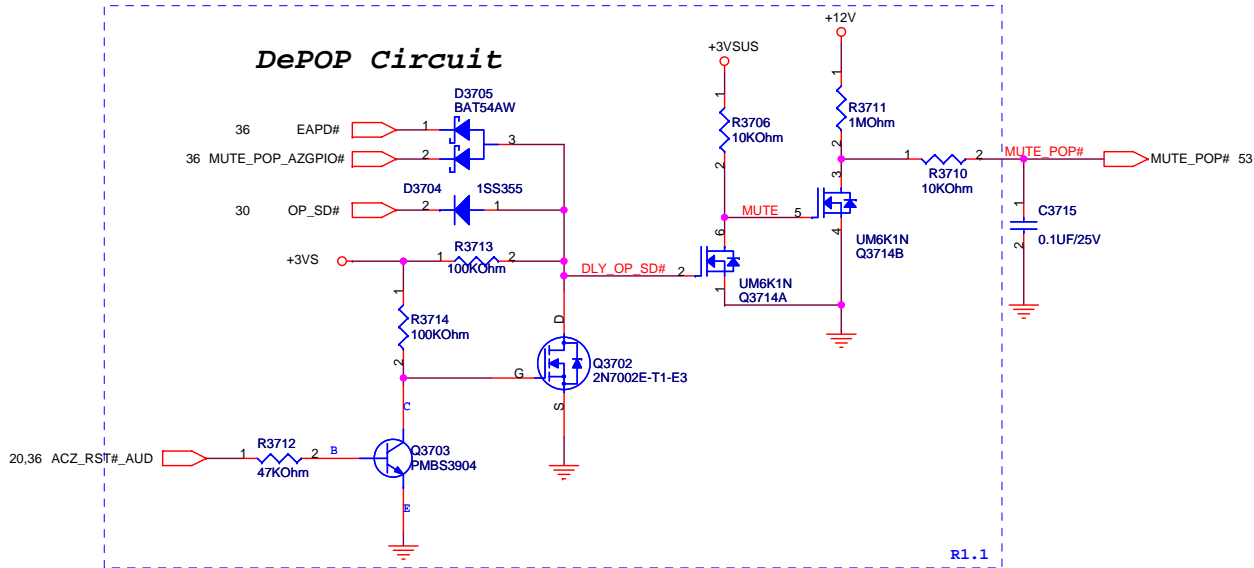
ASUS		Title : IO BRD CONN&DAA	
ASUSALPHA ODM NB1		Engineer: Warren	
Size	Project Name		
Custom	Rocky 30 IO Board		
Date: Monday, February 04, 2008	Sheet	33	of 94
	Rev	1.1	



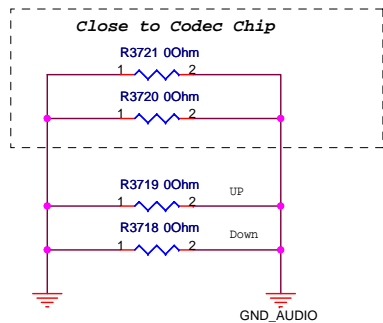
<Variant Name>		Title : LAN-RJ45	
ASUSTeK COMPUTER INC		Engineer: Warren	
Size	Project Name	Rocky 30 IO Board	
Custom		Rev 1.1	
Date: Monday, February 04, 2008		Sheet 35 of 94	



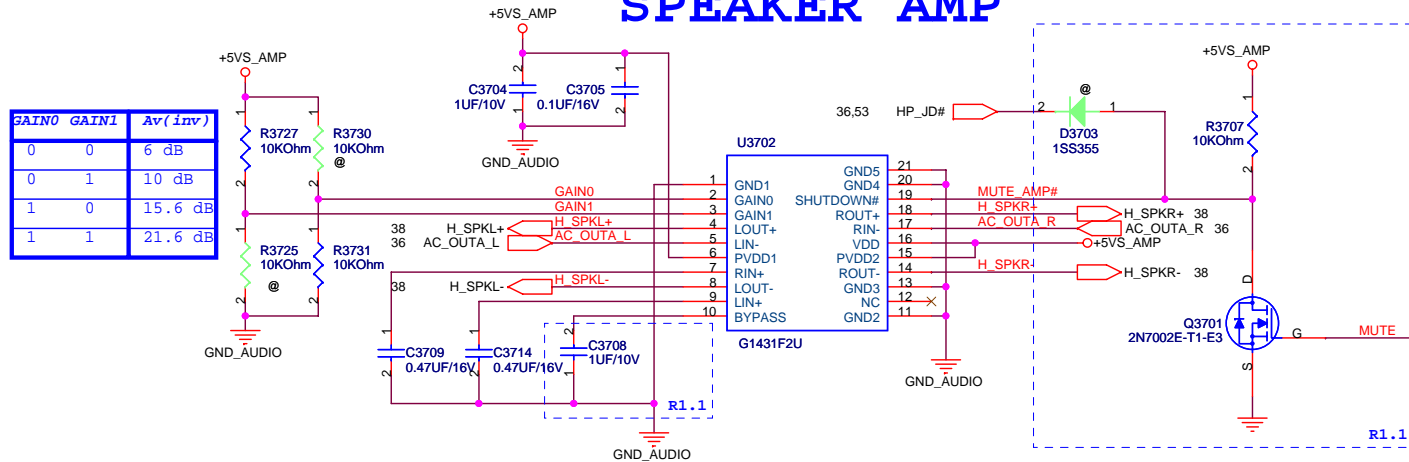
DePOP Circuit



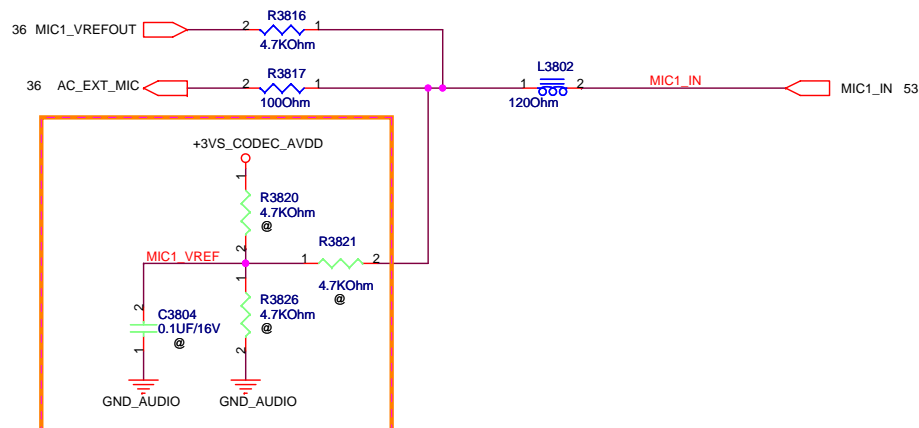
JACK GND



SPEAKER AMP

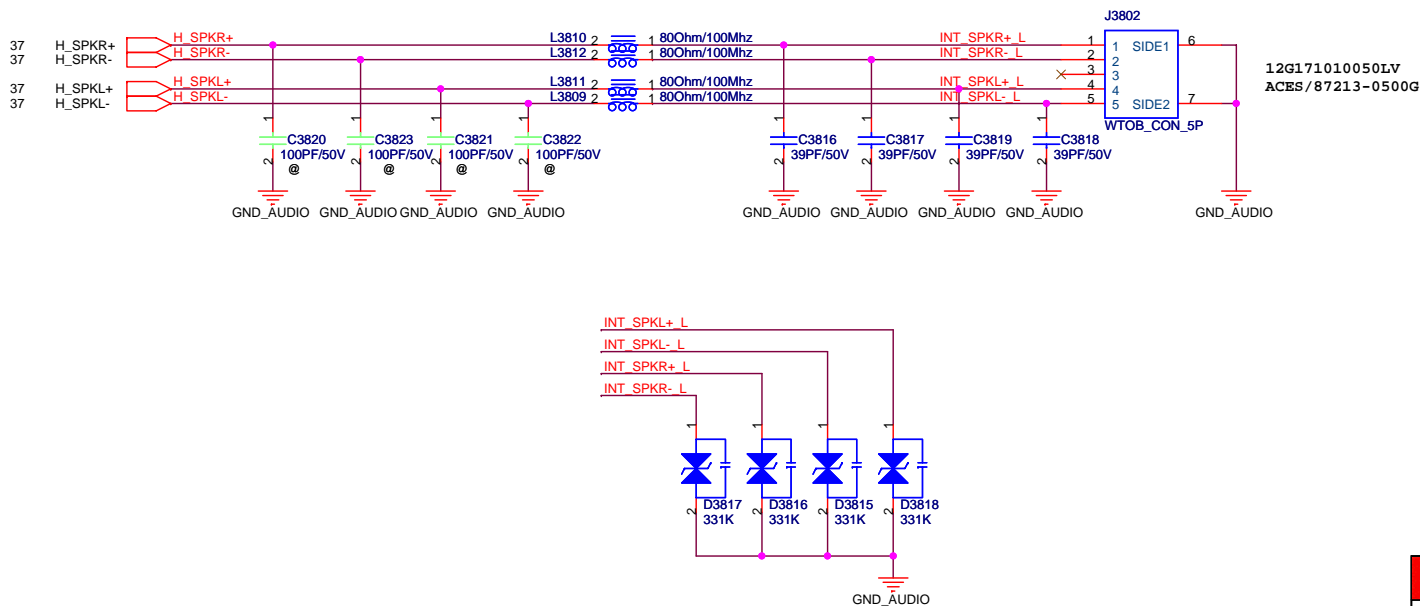


EXT MICROPHONE



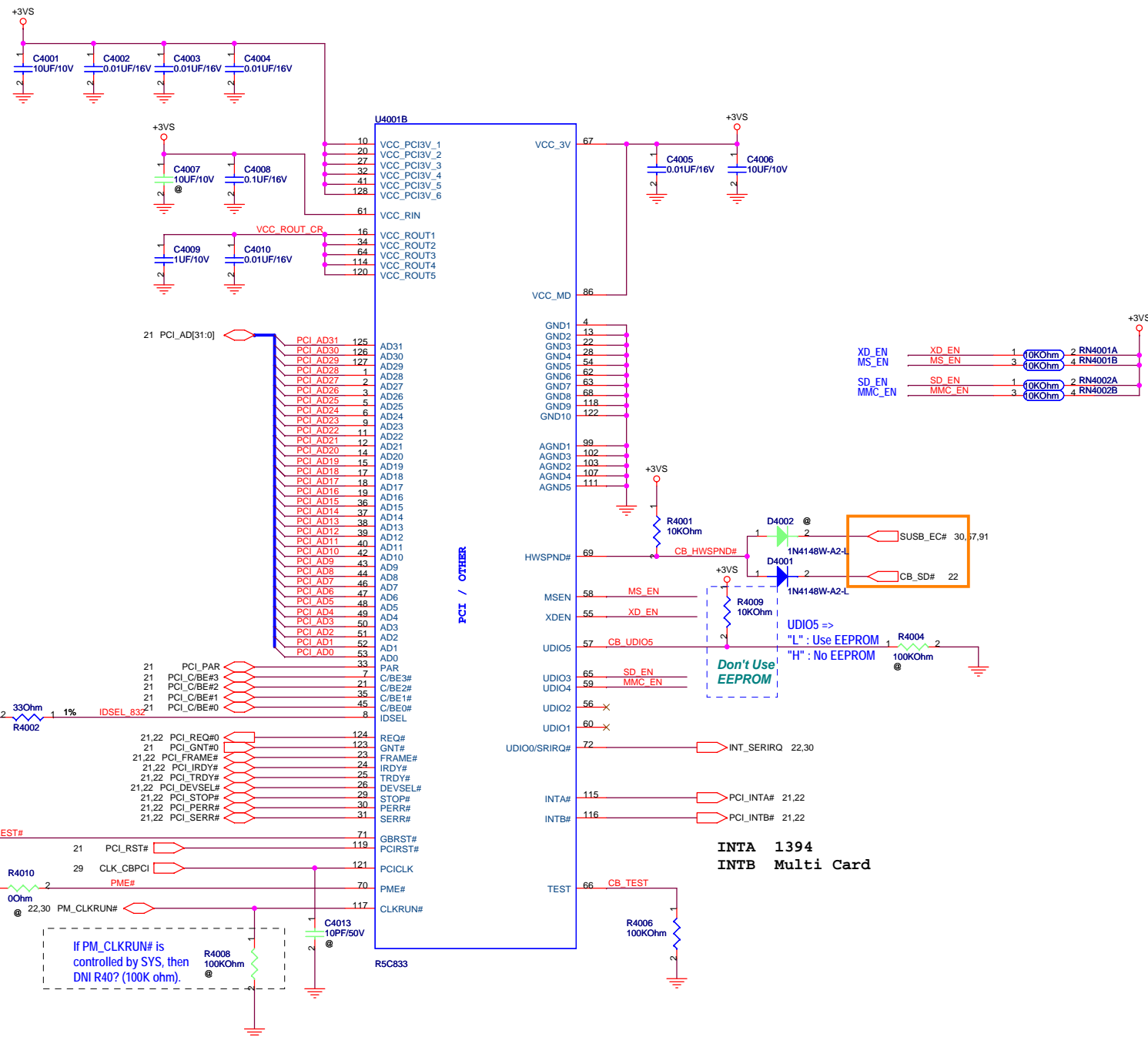
Reserved the external MIC bias(T filter).

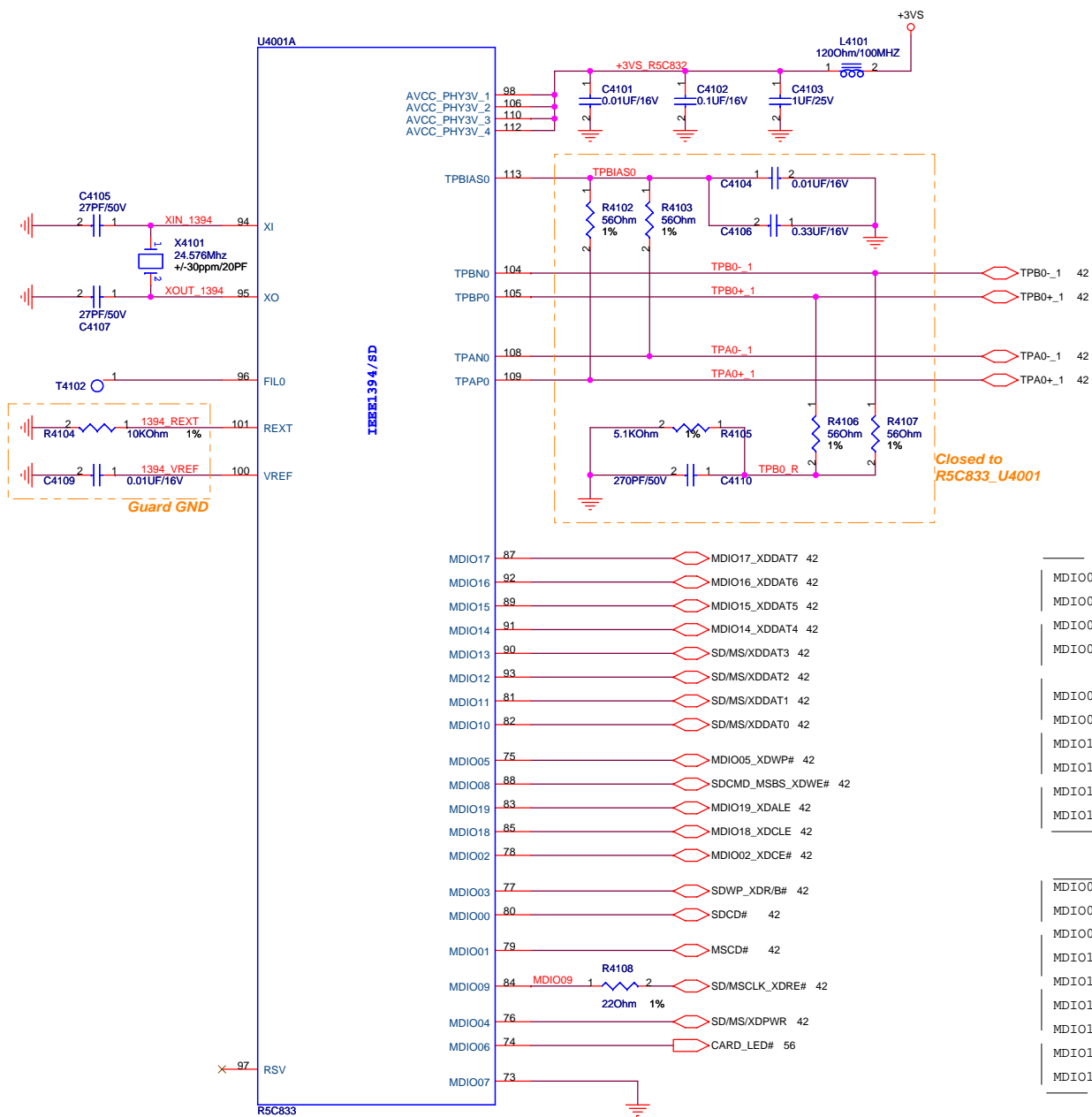
SPEAKER CONNECTOR



ASUS		Title : MIC&LINEIN	
Size B		Engineer: Peter Lo	
Project Name		Rev 1.0	
Date: Monday, February 04, 2008		Sheet 38 of 94	







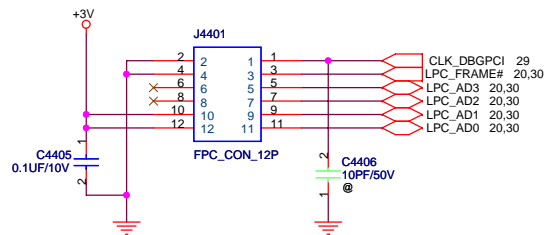
MDIO00-->	SD Card Detect
MDIO01-->	MS Card Detect
MDIO03-->	SD Write Protect
MDIO04-->	SD Card Power0 Control/ MS Power Control
MDIO08-->	SD Command/MS Bus State
MDIO09-->	SD Clock/MS Clock
MDIO10-->	SD Data 0/MS Data 0
MDIO11-->	SD Data 1/MS Data 1
MDIO12-->	SD Data 2/MS Data 2
MDIO13-->	SD Data 3/MS Data 3

MDIO02-->	xDCE#
MDIO05-->	SD Power Control 1 / xDWP
MDIO06-->	xD/MS/SD LED Control
MDIO14-->	xD Data
MDIO15-->	xD Data
MDIO16-->	xD Data
MDIO17-->	xD Data
MDIO18-->	xD CLE
MDIO19-->	xD ALE

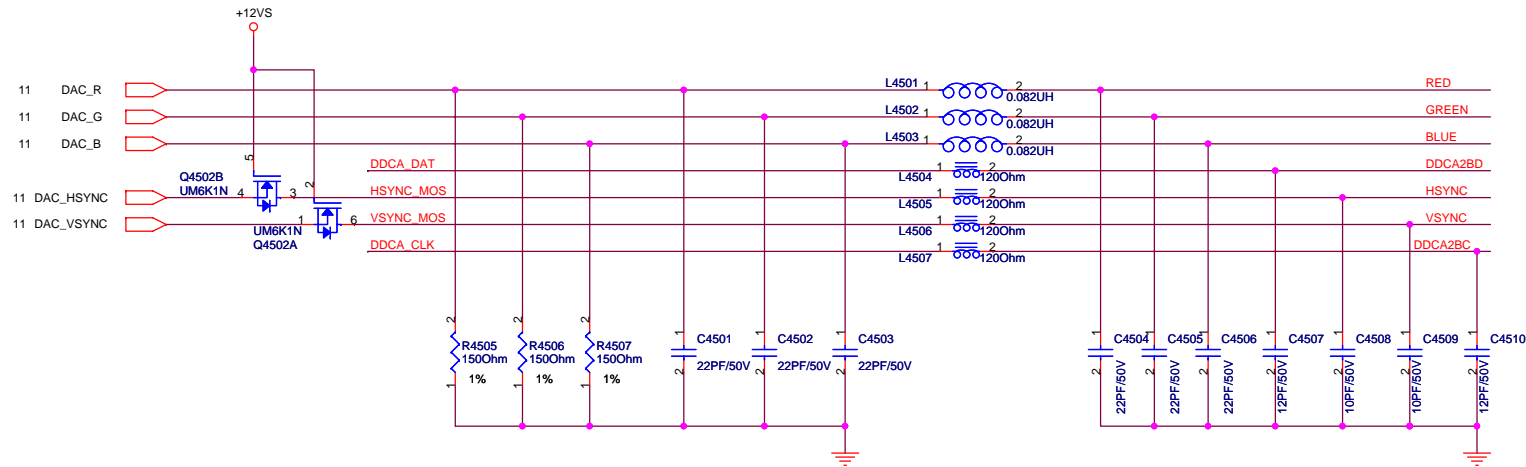


		Title : ****	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
Custom	Rocky30		1.0
Date: Thursday, October 18, 2007		Sheet	43 of 94

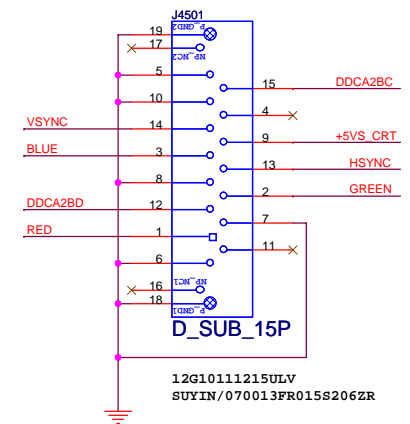
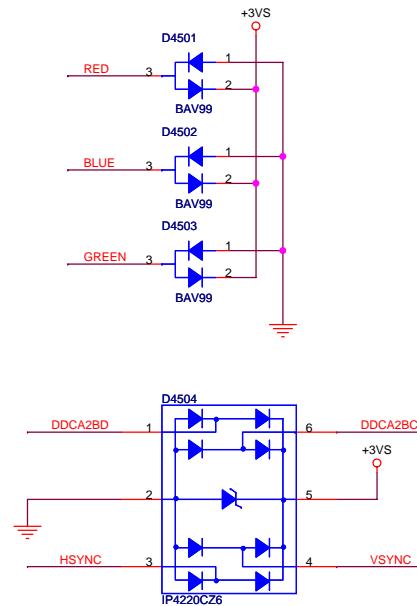
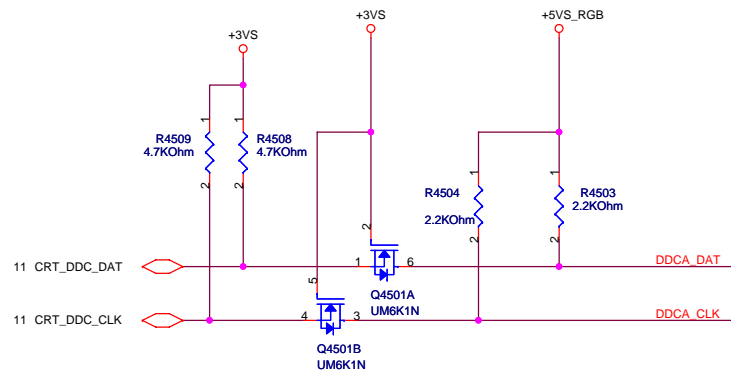
Block C

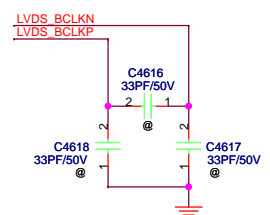
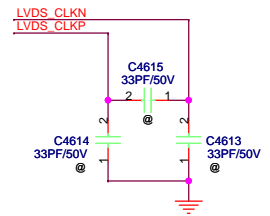
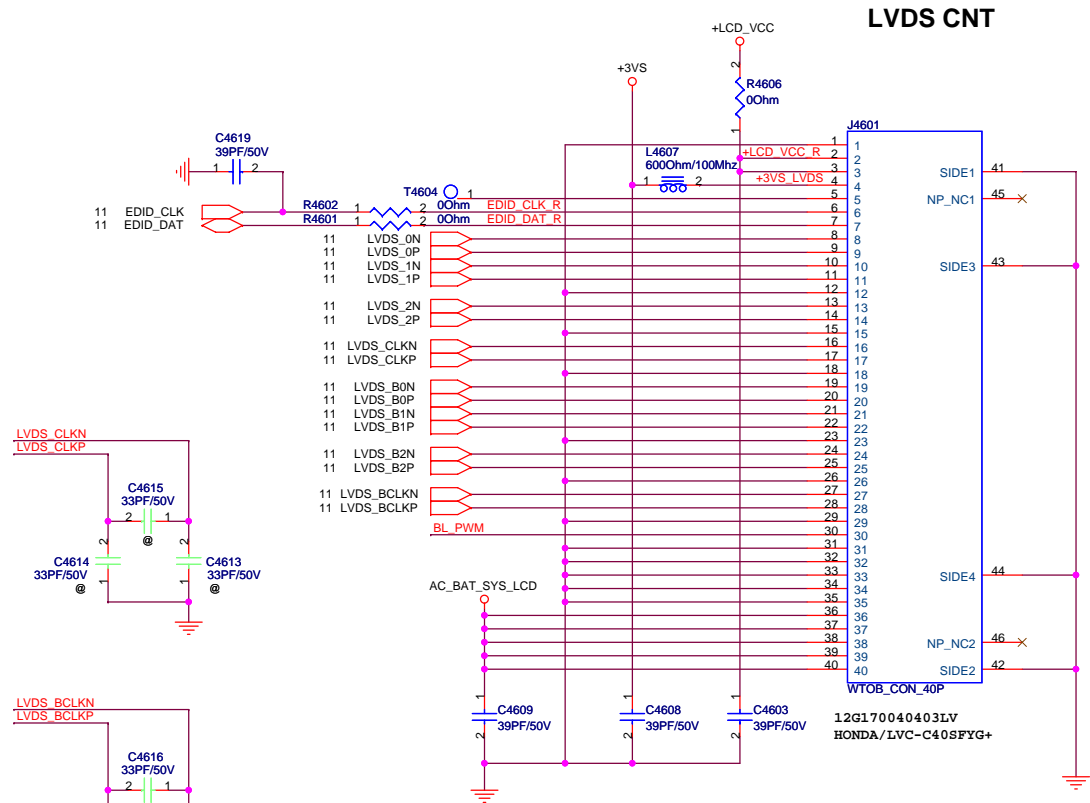


		Title : DEBUG	
Engineer: Peter Lo			
Size Custom	Project Name Rocky30		Rev 1.0
Date: Monday, February 04, 2008		Sheet 44 of 94	

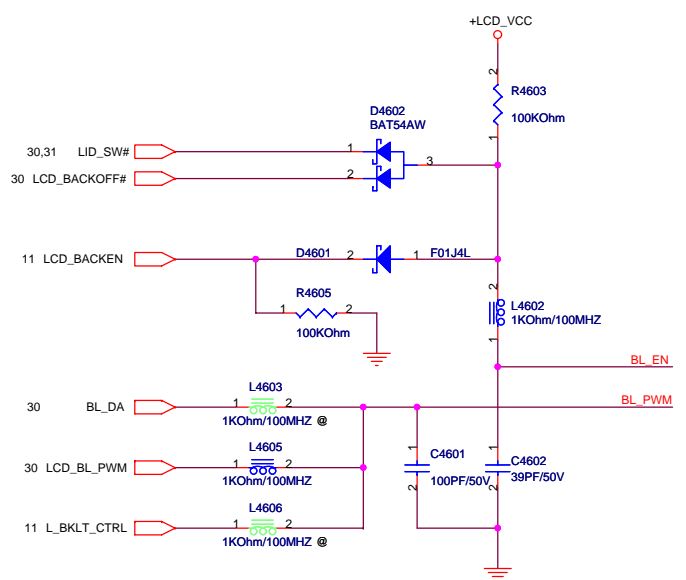
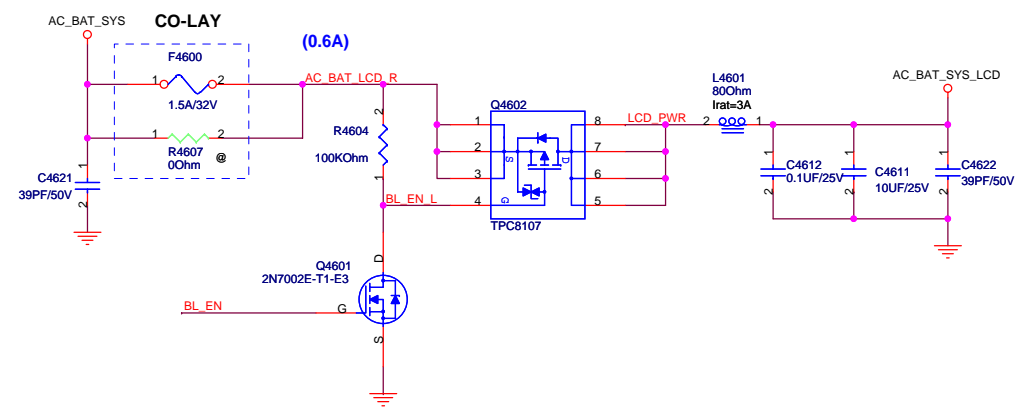
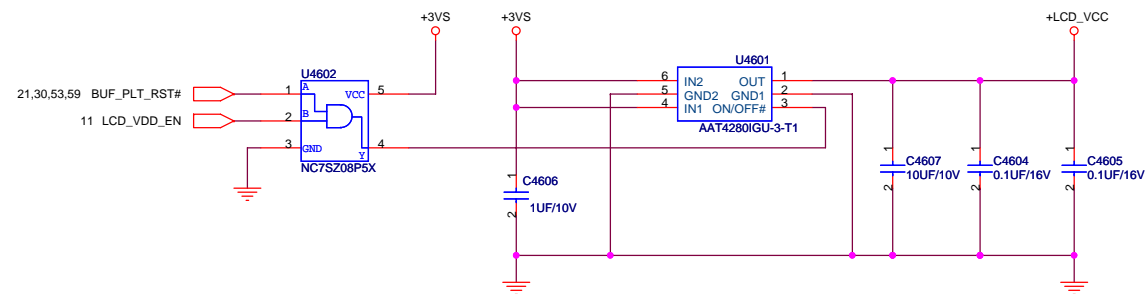


PLACE ESD Diodes near VGA port





Power Switch for LCD Power

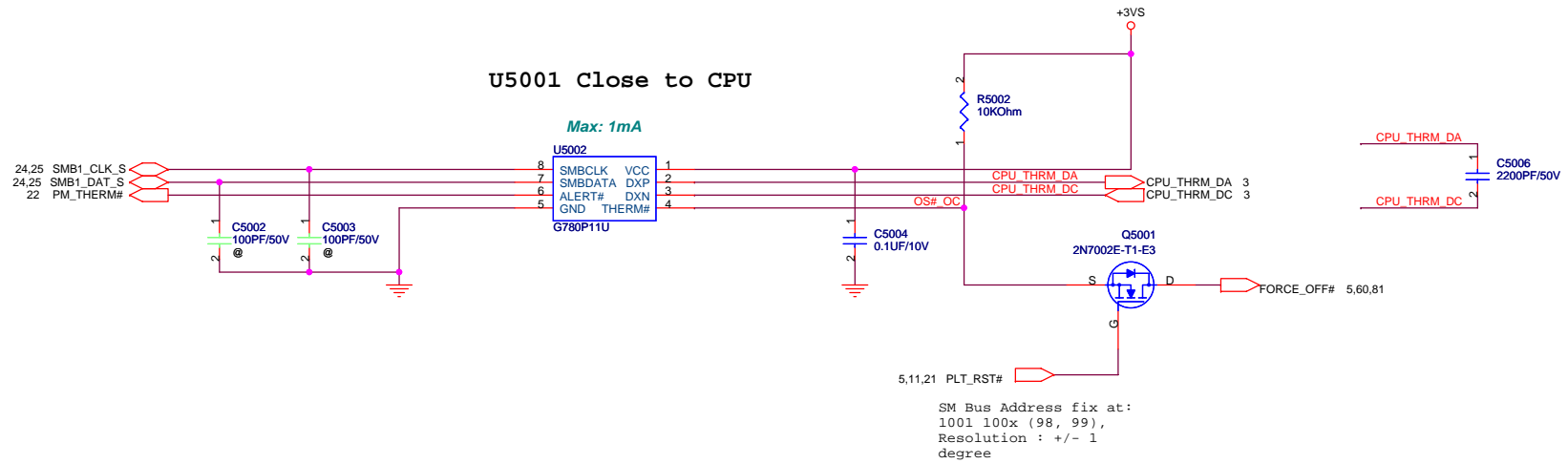




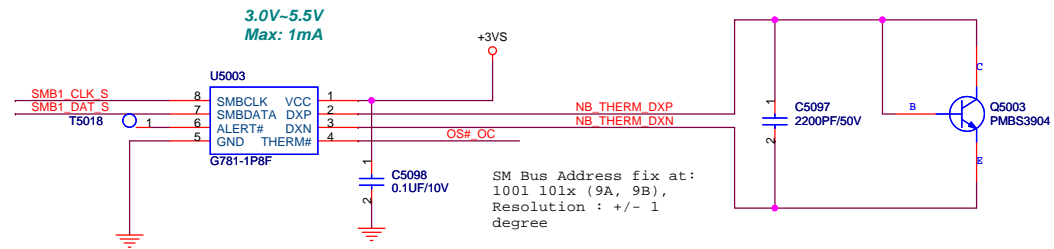
	5	4	3	2	1
D					D
C					C
B					B
A					A
<div>ASUS®</div> <div>Title :</div>					
Engineer: <i>Peter Lo</i>					
Size A	Project Name Rocky30				Rev 1.0
Date: <i>Thursday, October 18, 2007</i>				Sheet	49 of 94

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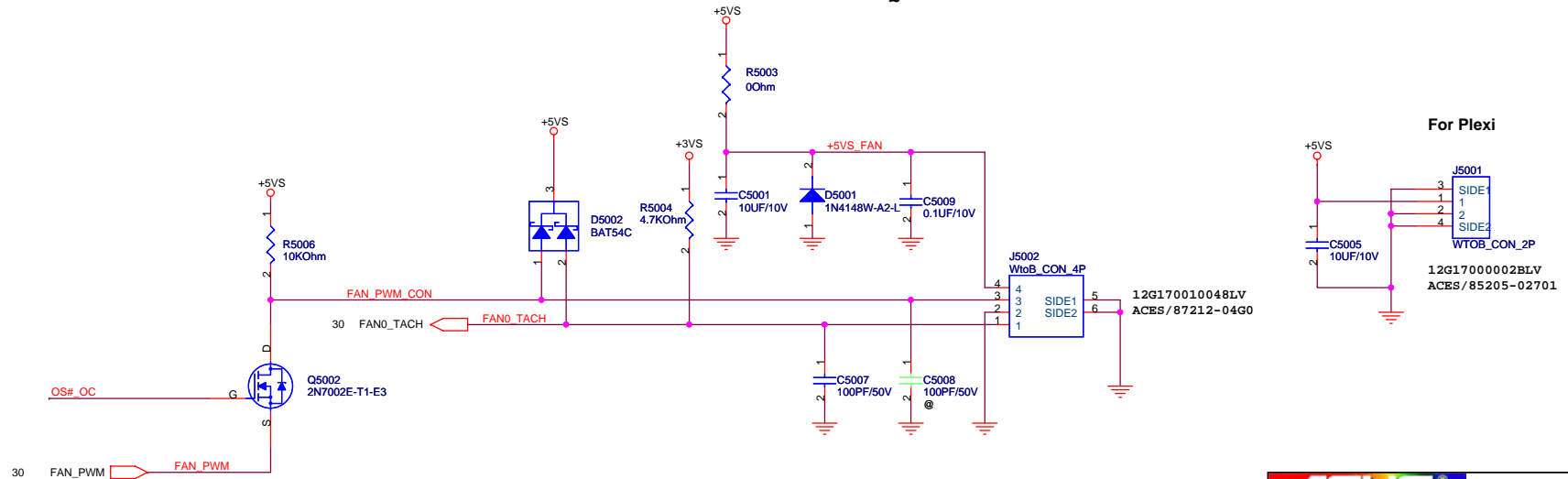
Thermal Sensor

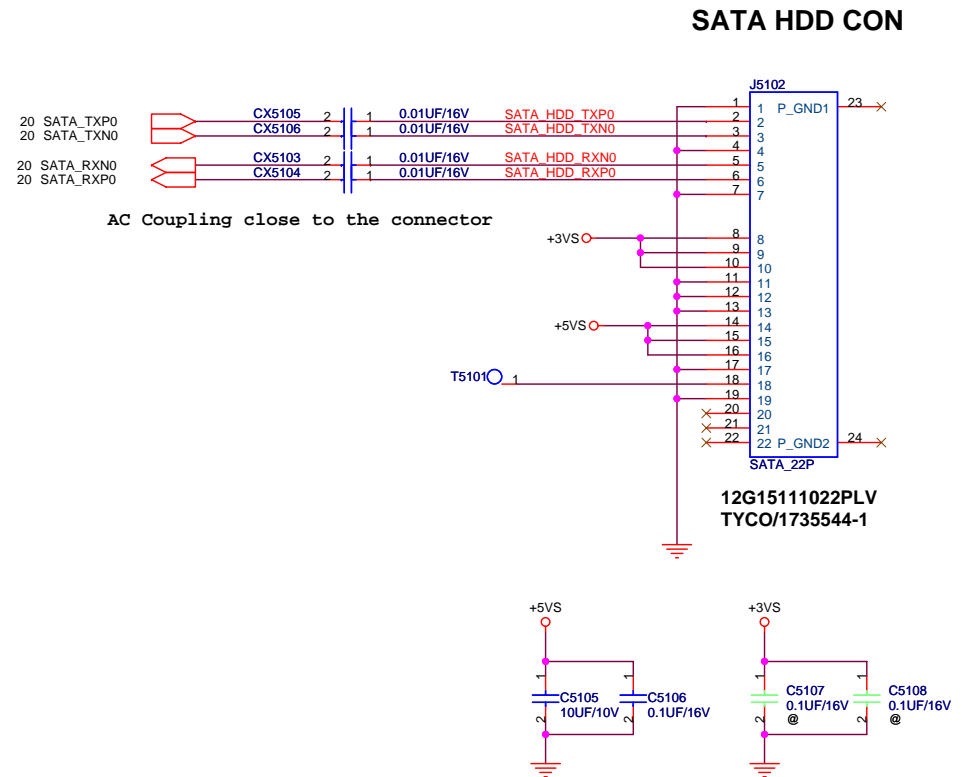
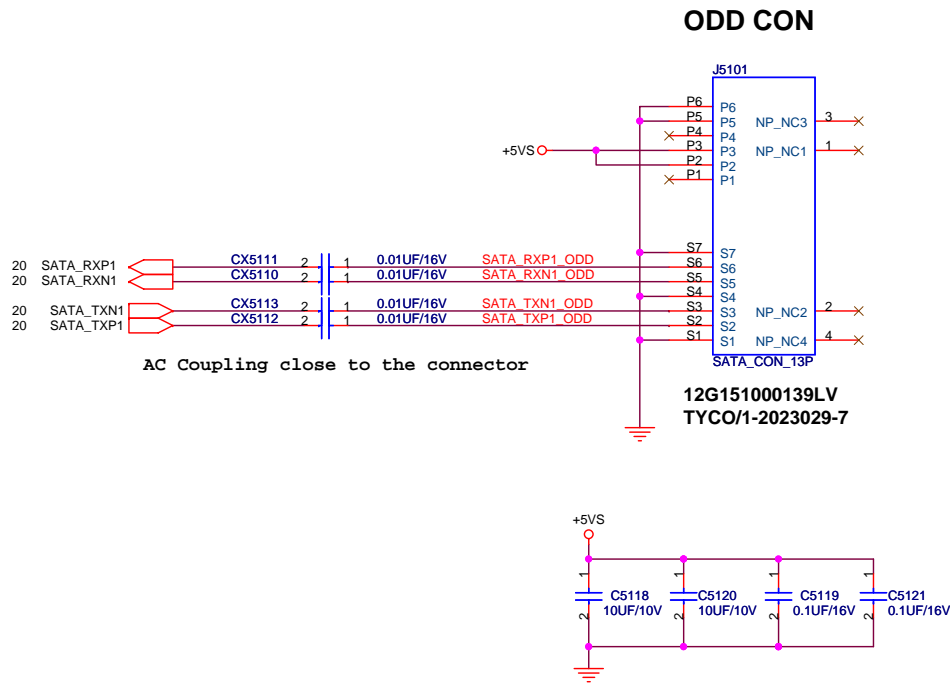


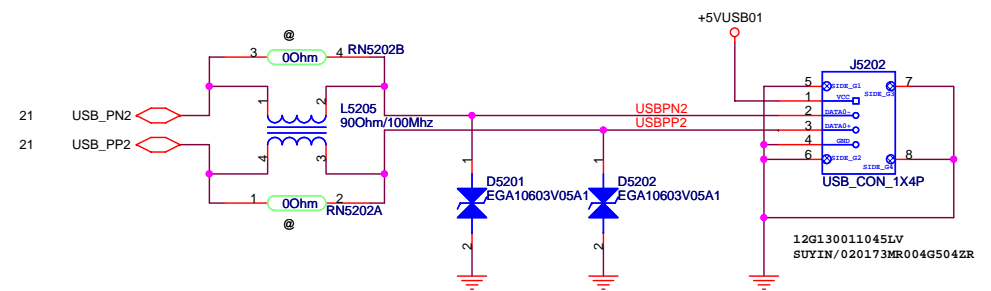
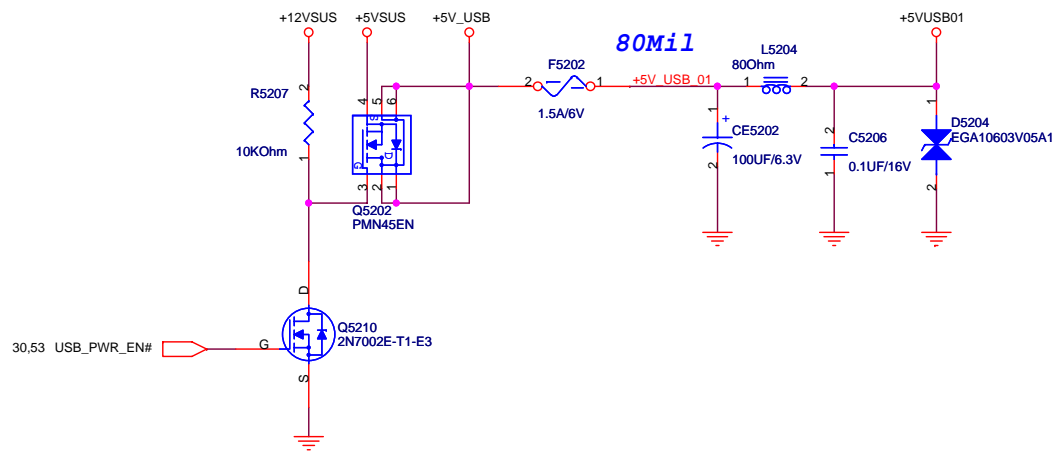
U5003 Close to SB and DIMM (Remove after DV stage)



Q5003 Close to NB

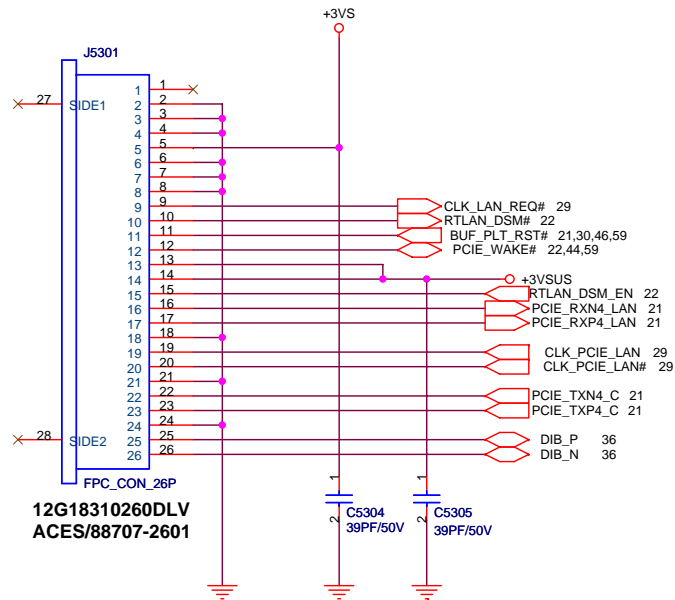




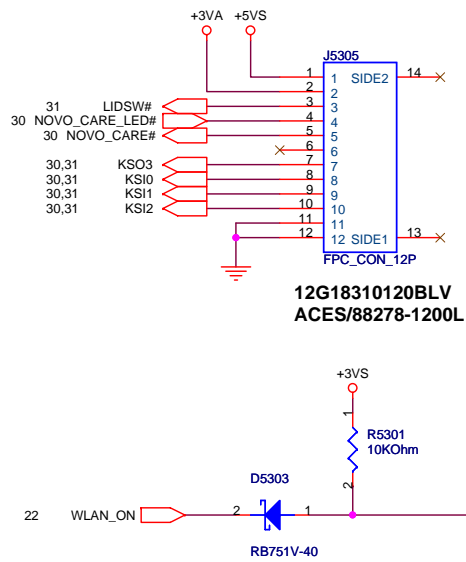


ASUS		Title : USB CONN	
		Engineer: Peter Lo	
Size B	Project Name Rocky30		Rev 1.0
Date: Monday, February 04, 2008		Sheet 52 of 94	

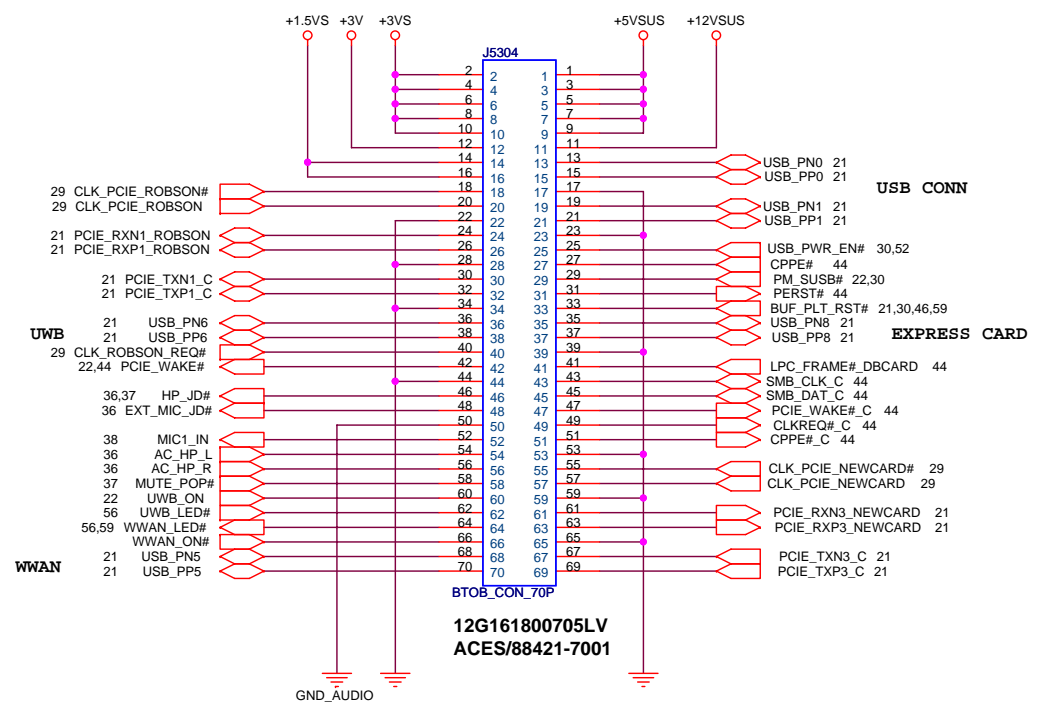
IO BOARD



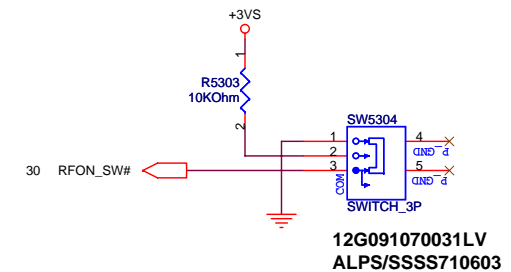
For Media Control Board



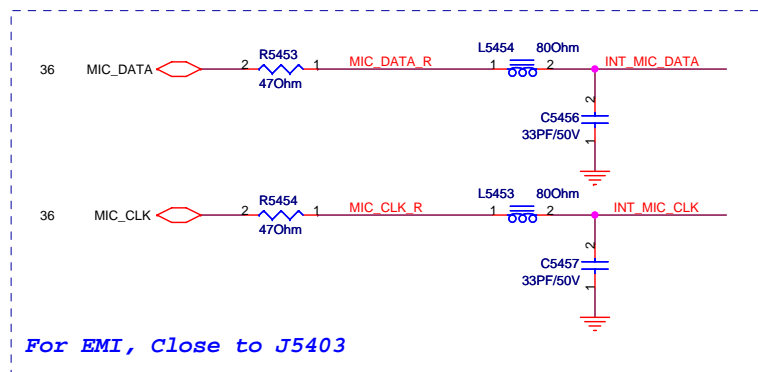
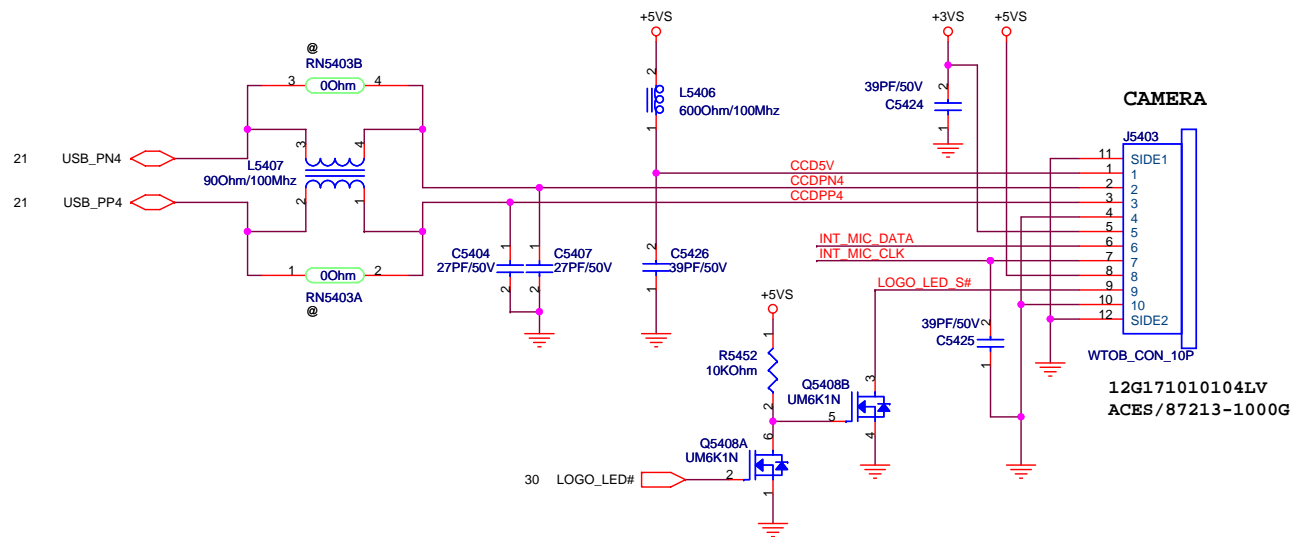
SMALL BOARD



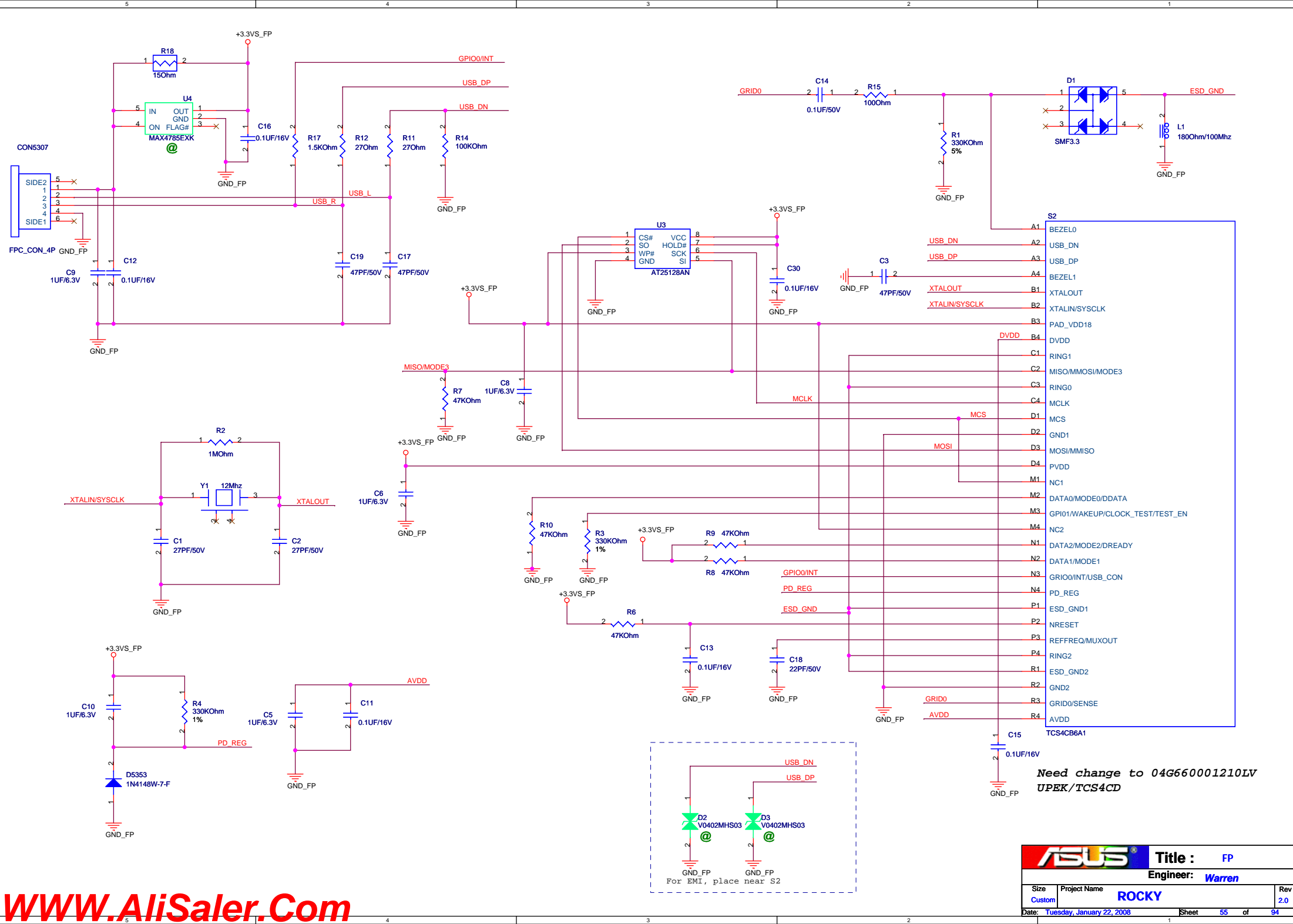
Wireless Switch



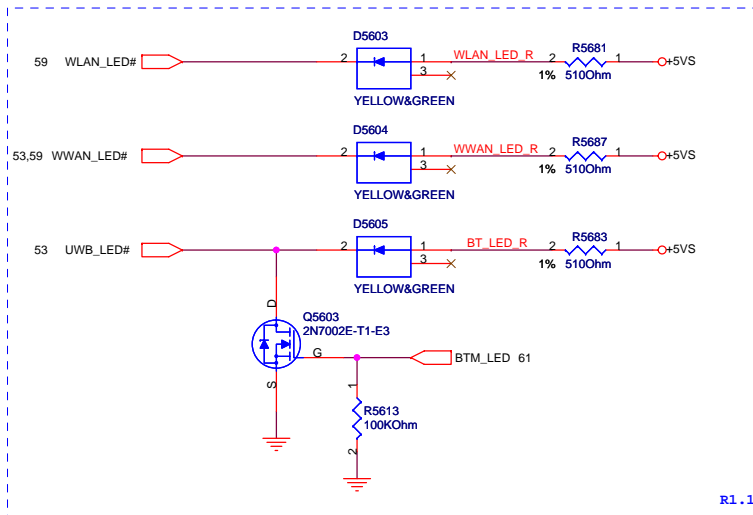
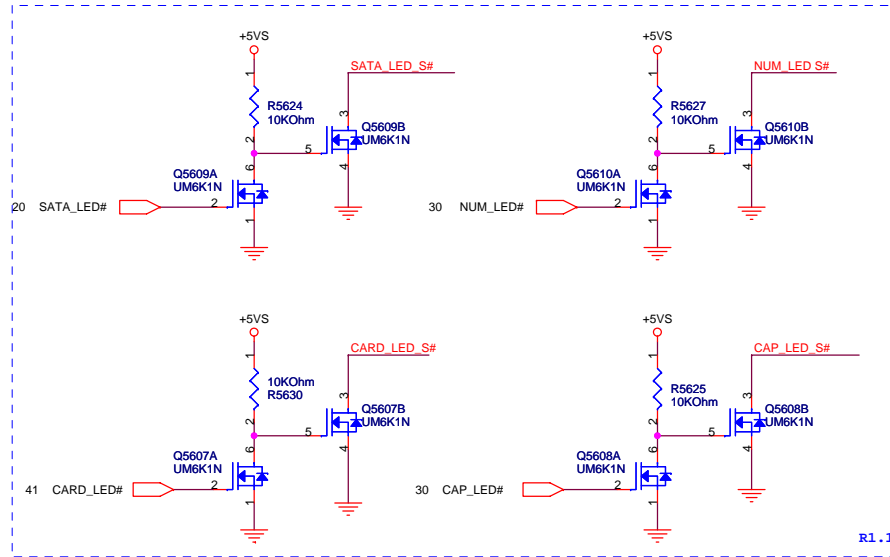
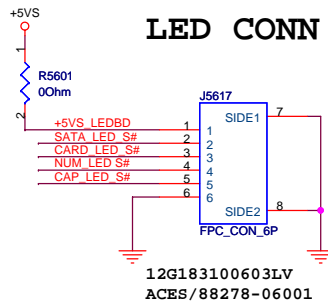
ASUS			Title : IO BOARD	
			Engineer: Peter Lo	
Size B	Project Name Rocky30			Rev 1.0
Date: Monday, February 04, 2008		Sheet 53 of 94		



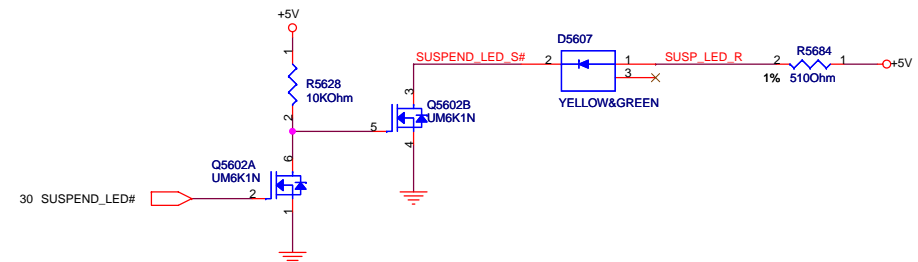
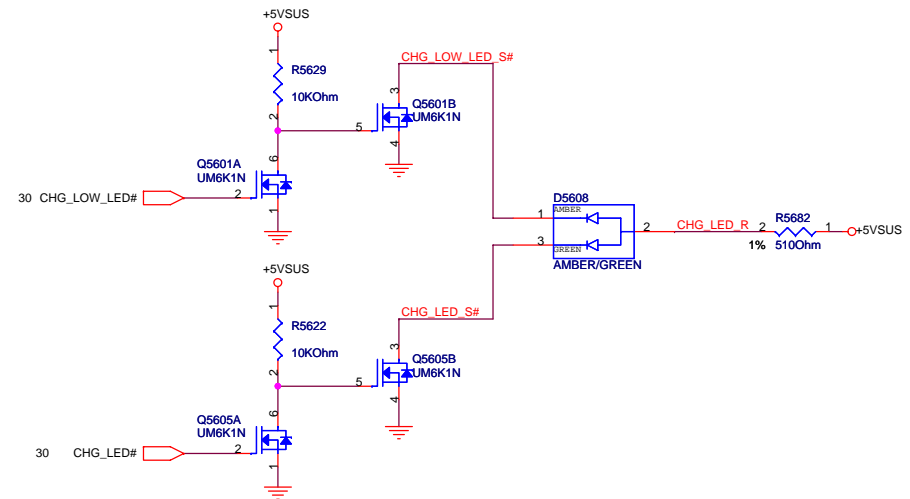
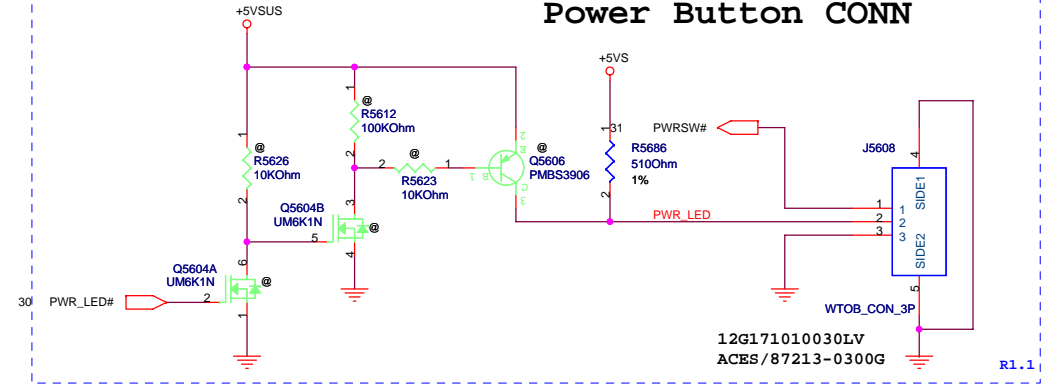
ASUS		Title : CAMERA	
		Engineer: Peter Lo	
Size	Project Name	Rev	
B	Rocky30	1.0	
Date: Monday, February 04, 2008		Sheet	54 of 94

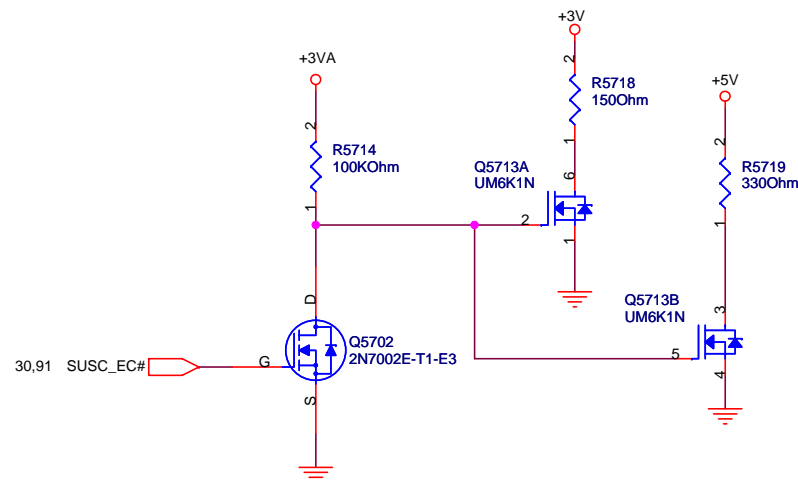
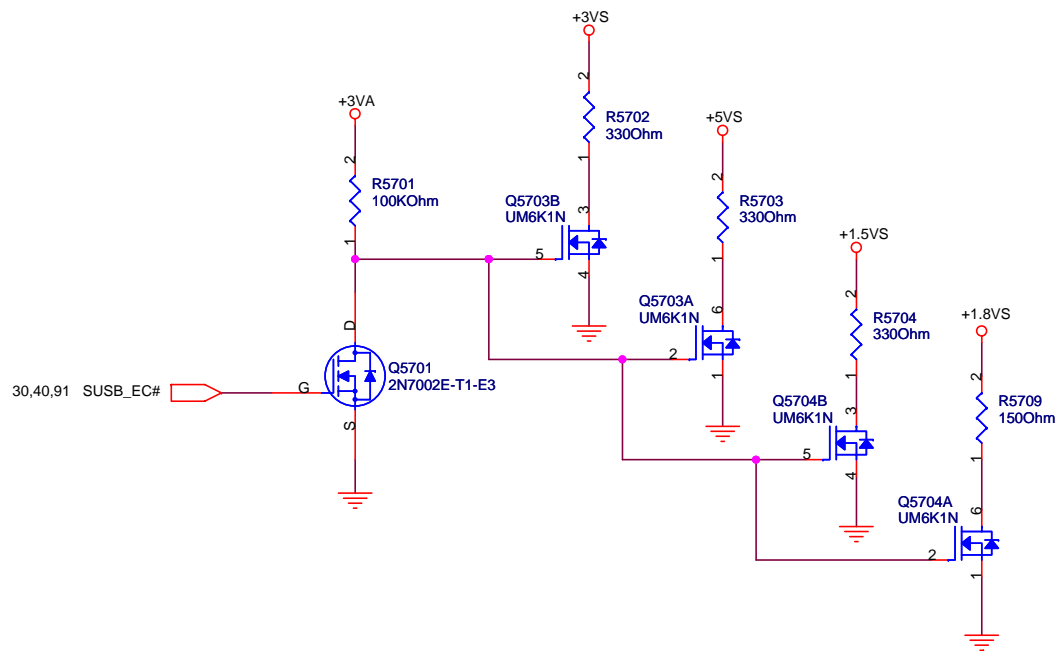


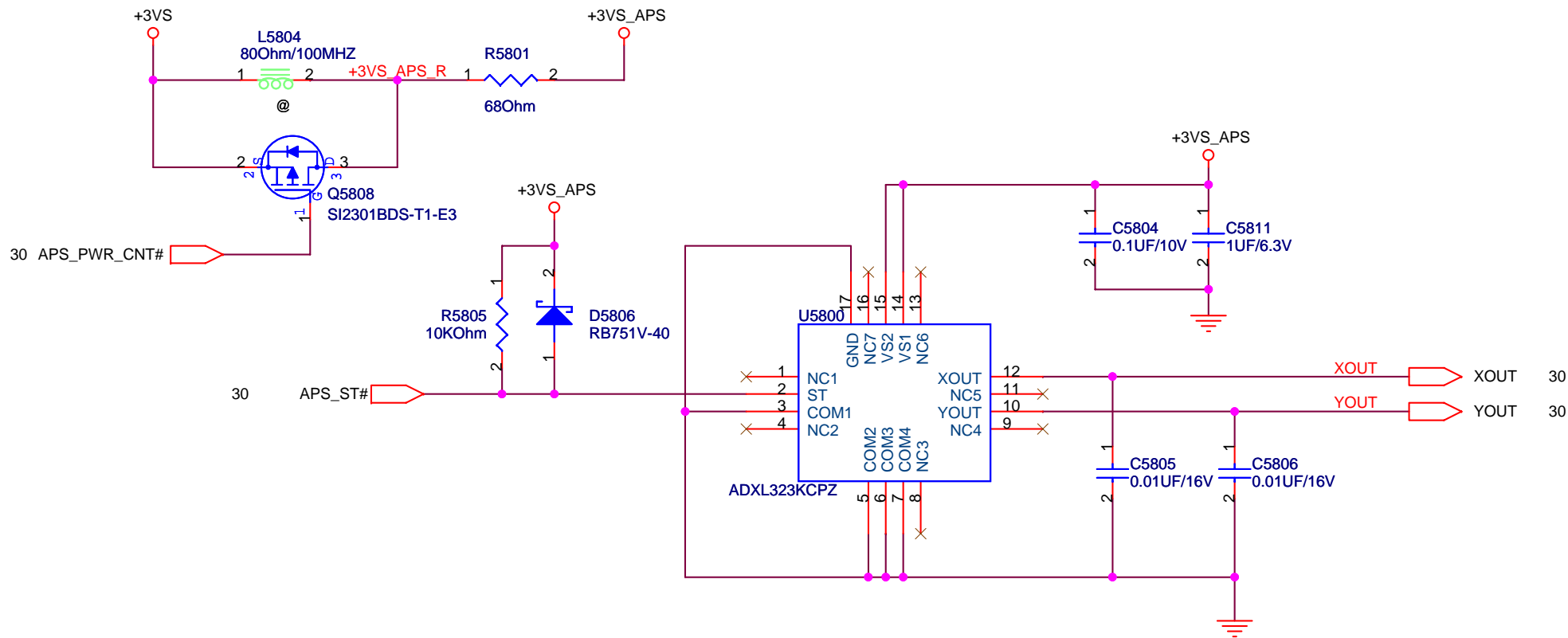
LED CONN



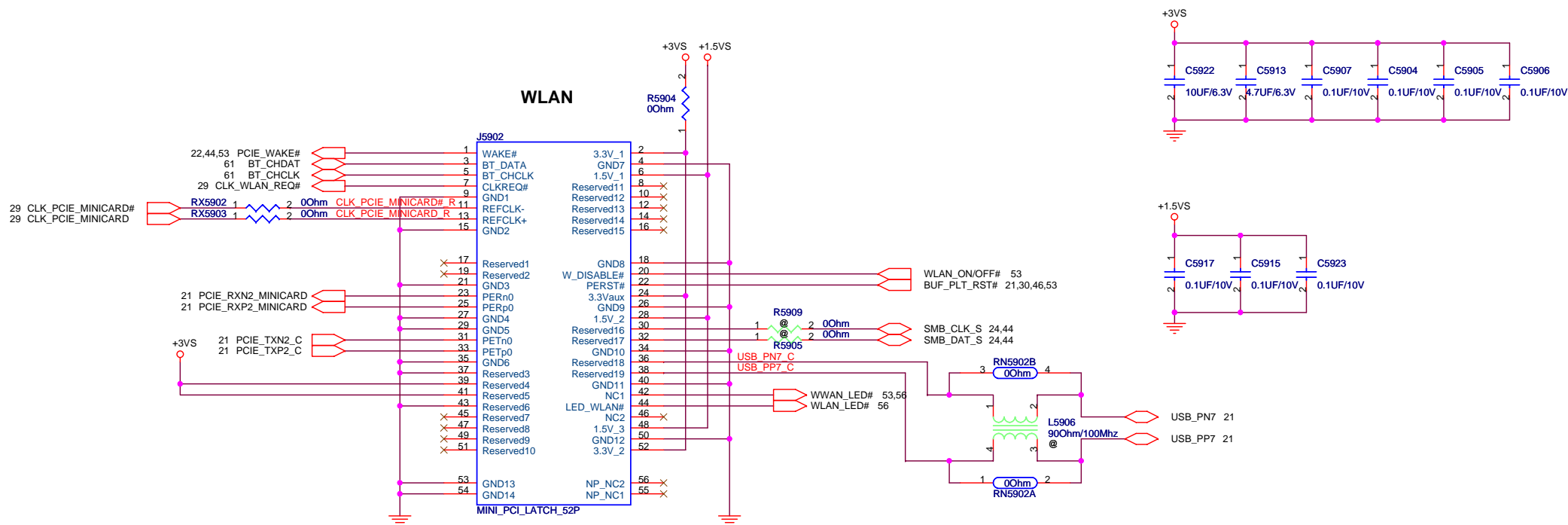
Power Button CONN





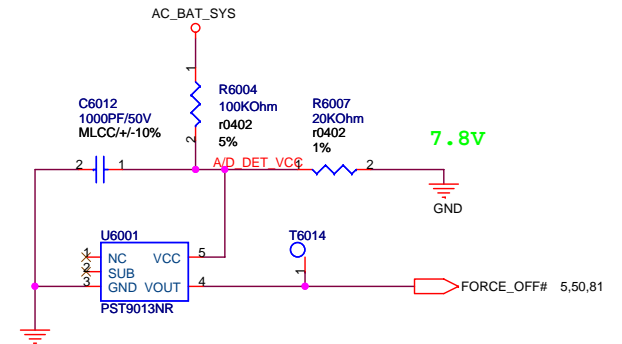
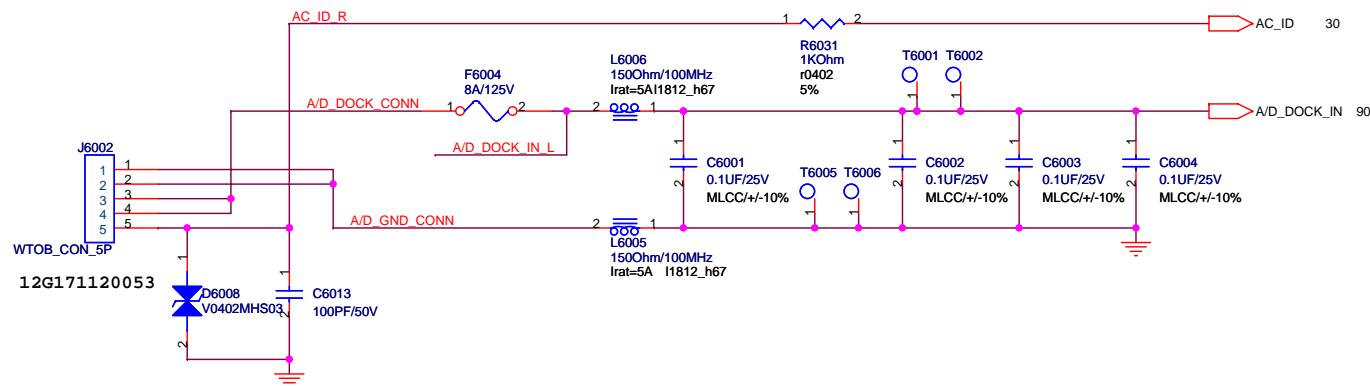


ASUS		Title : SMS	
		Engineer: Peter Lo	
Size A	Project Name Rocky30		Rev 1.0
Date: Monday, February 04, 2008		Sheet 58 of 94	



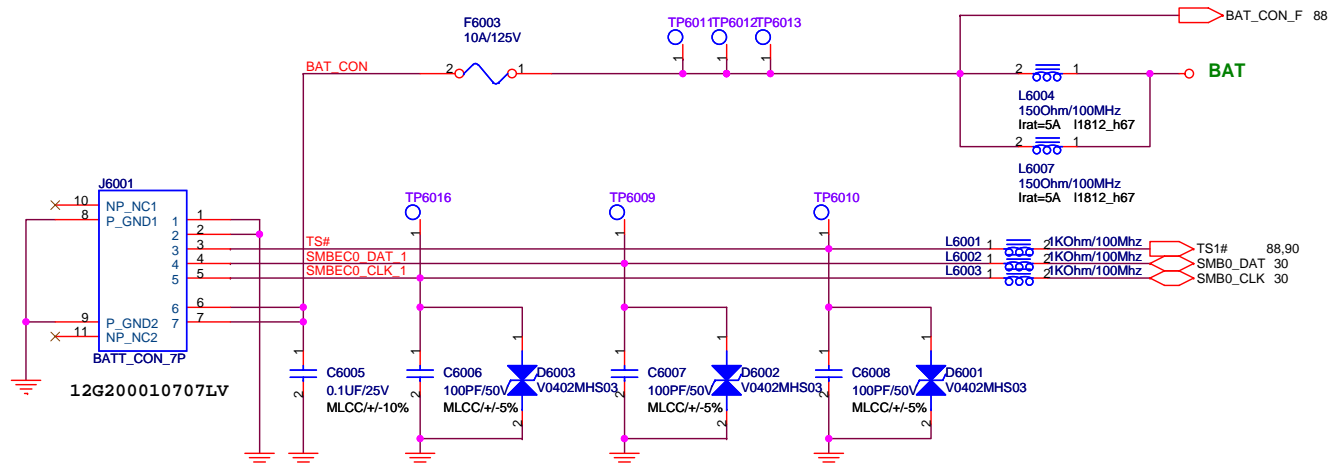
ASUS		Title : Mini Card	
		Engineer: Peter Lo	
Size B	Project Name Rocky30	Rev 1.0	
Date: Monday, February 04, 2008		Sheet 59 of 94	

DC IN CONN



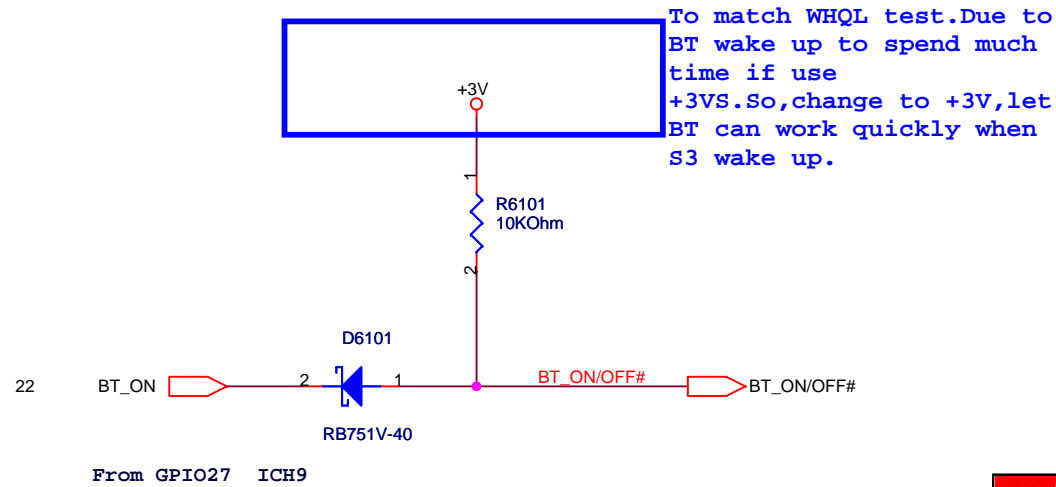
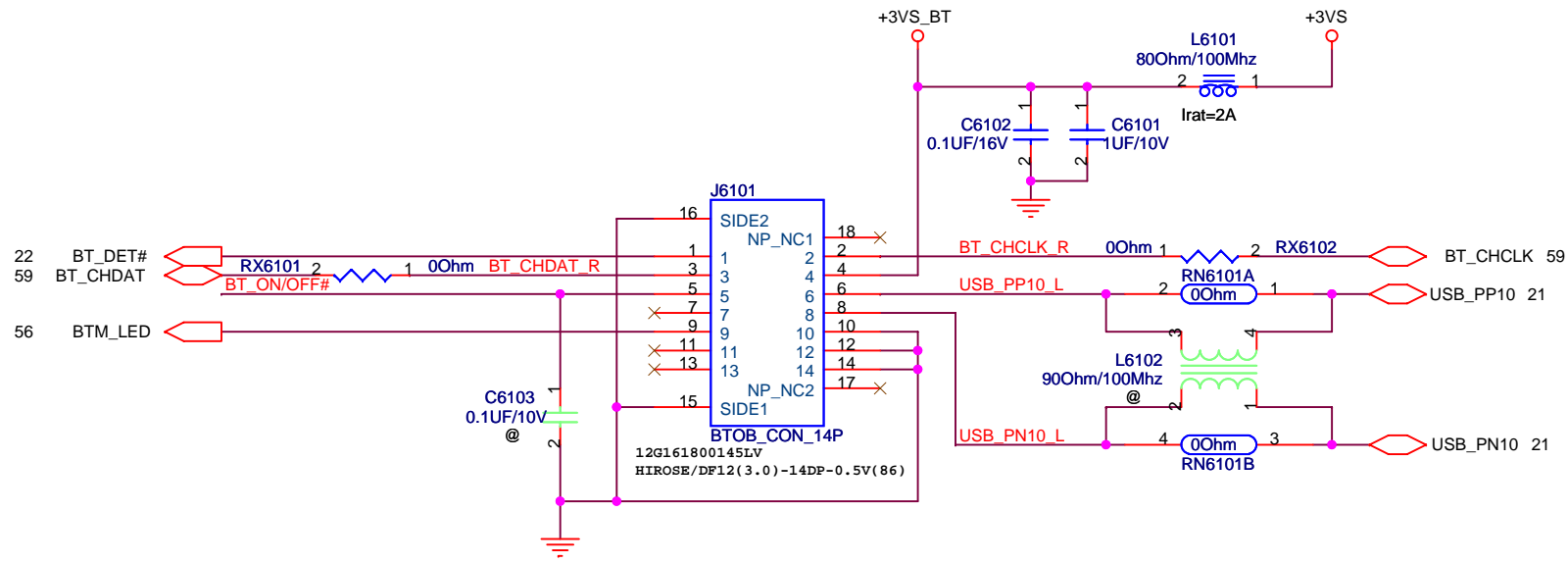
Without Battery & Pull out Adapter

Battery CONN



ASUS		Title : DC Jack & Battery CONN	
		Engineer: Kevin Chang	
Size	Project Name	Rocky 30	Rev 1.0
Custom			
Date: Monday, February 04, 2008		Sheet	60 of 94


Blue Tooth




To match WHQL test.Due to BT wake up to spend much time if use +3V,let BT can work quickly when S3 wake up.

ASUS		Title : BlueTooth	
		Engineer: Peter Lo	
Size A4	Project Name Rocky30		Rev 1.0
Date: Monday, February 04, 2008		Sheet 61	of 94

5	4	3	2	1
D				
C				
B				
A				

		Title : ***	
Engineer: Peter Lo			
Size	Project Name		Rev
A4	Rocky30		1.0
Date: Thursday, October 18, 2007		Sheet	62 of 94

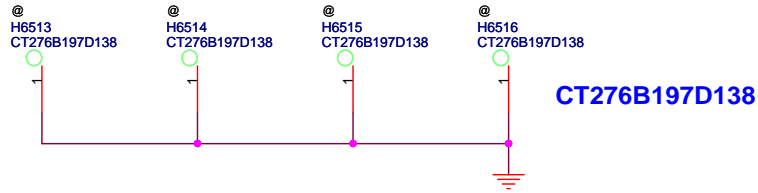
5	4	3	2	1
D				
C				
B				
A				

		Title : ***	
Engineer: <i>Peter Lo</i>			
Size	Project Name		Rev
A4	Rocky30		1.0
Date: Thursday, October 18, 2007		Sheet	63 of 94

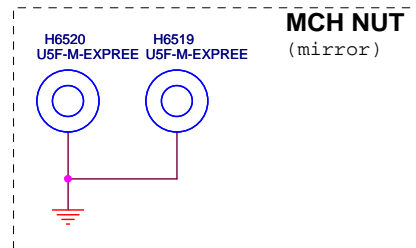
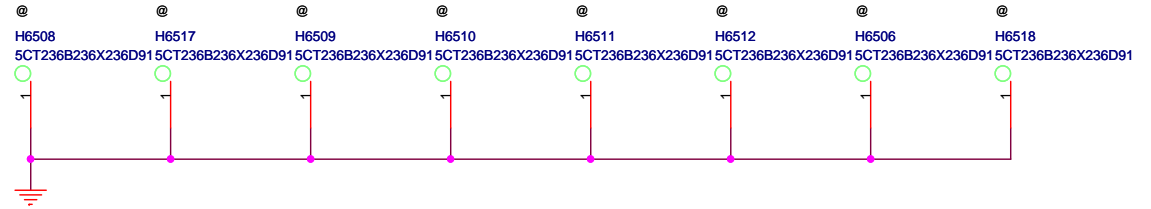
5	4	3	2	1
D				D
C				C
B				B
A				A
<div>ASUS®</div> <div>Title :</div>				
Engineer: <i>Peter Lo</i>				
Size	Project Name			Rev
A	Rocky30			1.0
Date: <i>Thursday, October 18, 2007</i>			Sheet <i>64</i> of <i>94</i>	

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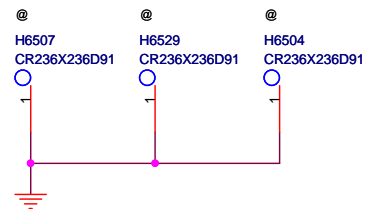
CPU



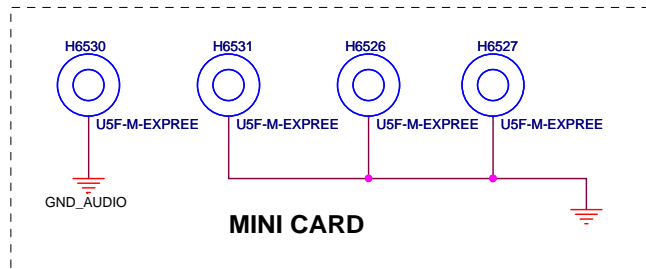
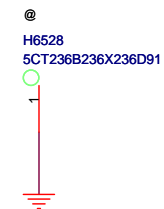
TOP 5CT236B236X236D91 PTH



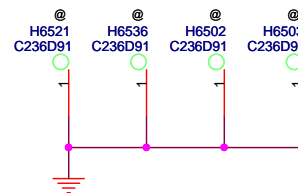
CR236X236D91 PTH



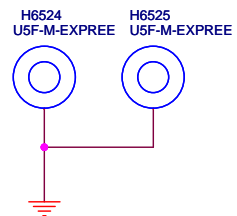
BOT 5CT236B236X236D91 PTH



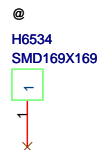
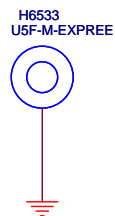
C236D91 PTH



For Fan Stand Off
C236B189D150 PTH (mirror)



For KB Stand Off
C236B189D150 PTH

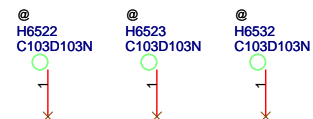


For BT StandOff




TOOLING HOLE

For ICT




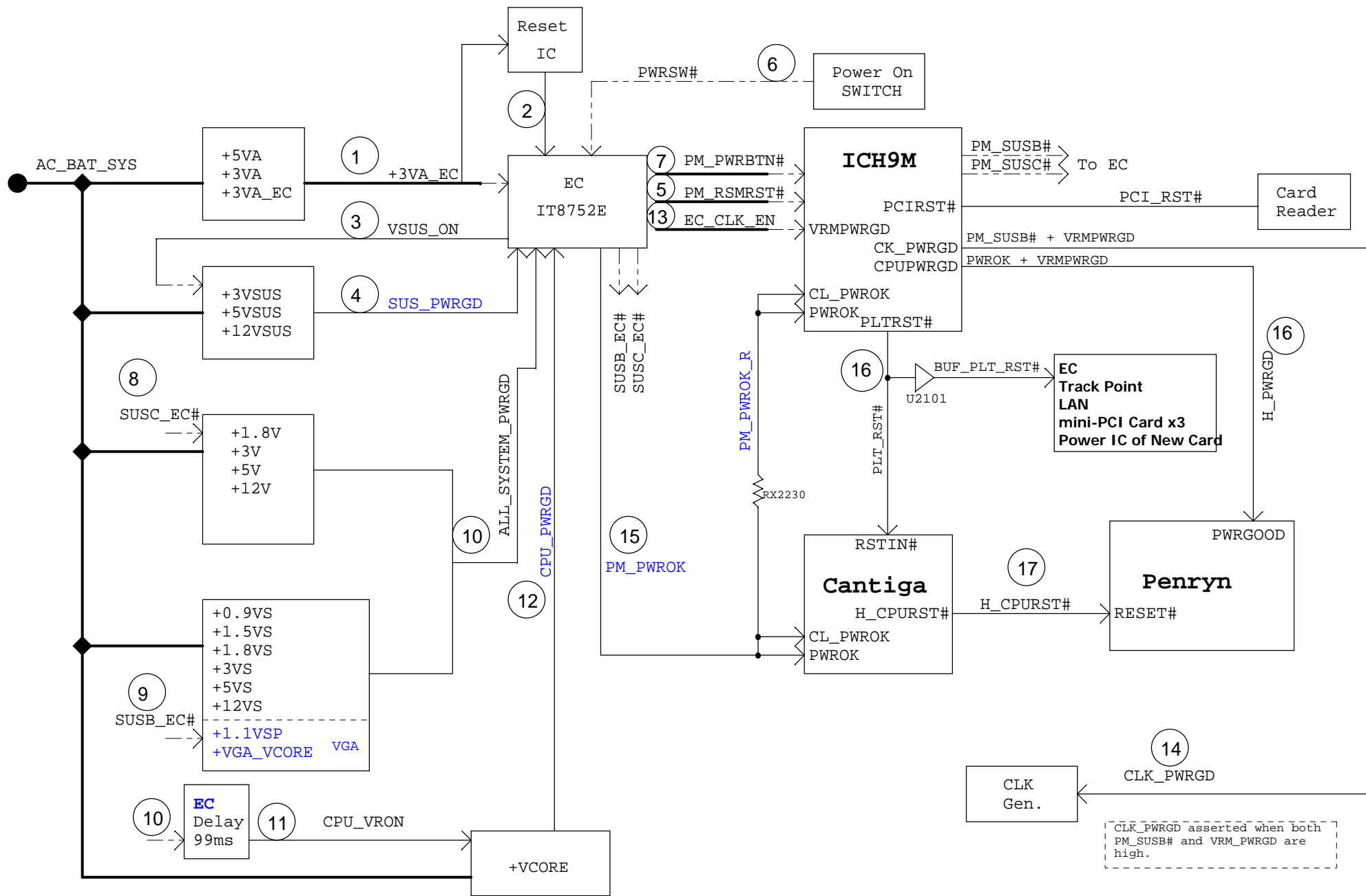
ASUS		Title MDC NUT & Hinksink NUT	
		Engineer: Peter Lo	
Size Custom	Project Name Rocky30		Rev 1.0
Date: Tuesday, January 22, 2008		Sheet 65 of 94	

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
Custom	Rocky30		1.0
Date: Thursday, October 18, 2007		Sheet	66 of 94





		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
Custom	Rocky30		1.0
Date: Thursday, October 18, 2007		Sheet	68 of 94



Power On Sequence



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>70</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>71</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>72</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>73</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>74</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>75</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>76</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

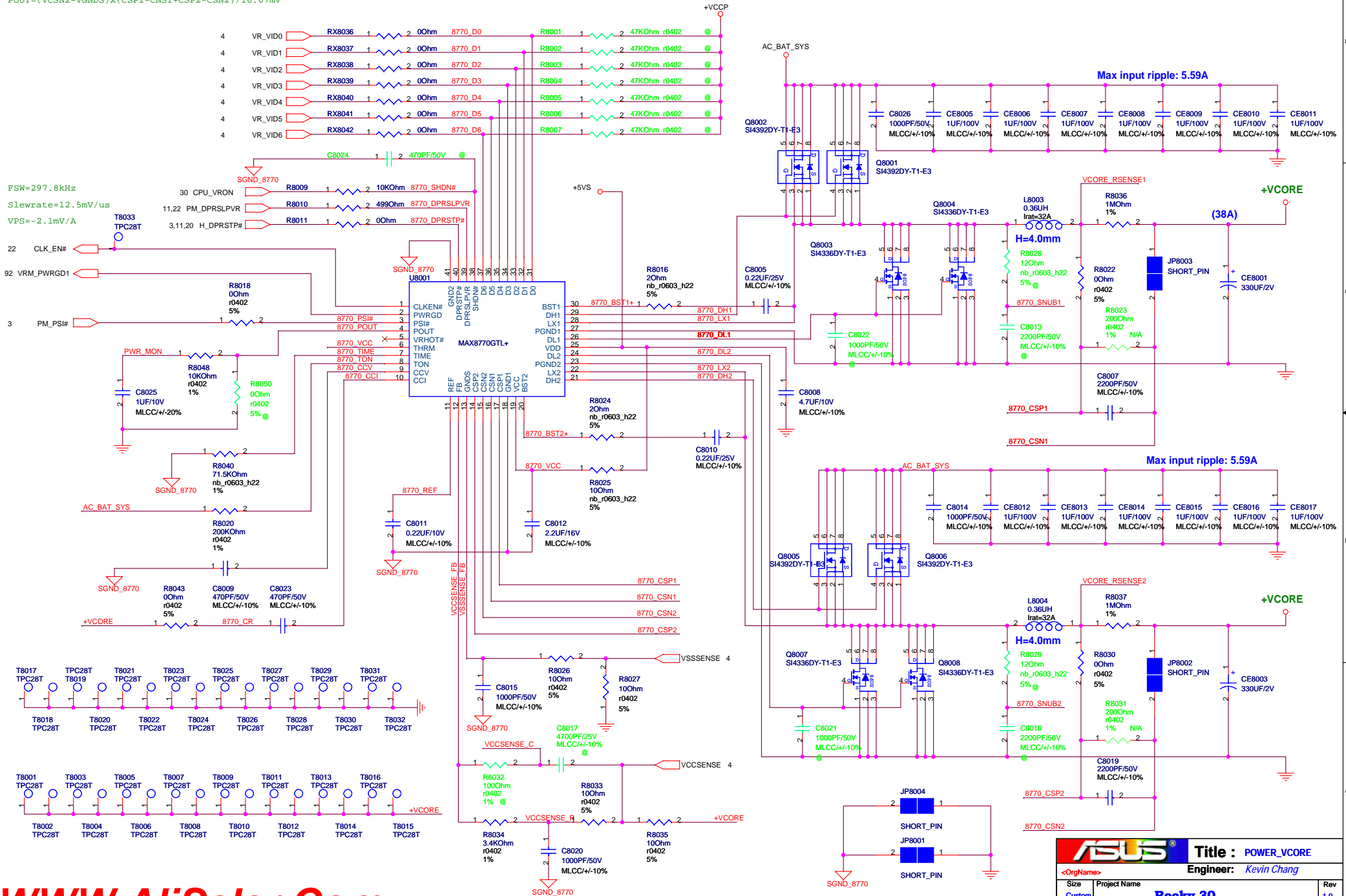
		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>77</i> of <i>94</i>	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size B	Project Name Rocky30		Rev 1.0
Date: <i>Thursday, October 18, 2007</i>		Sheet <i>78</i> of <i>94</i>	

	5	4	3	2	1
D					D
C					C
B					B
A					A
<div>WWW.AliSaler.Com</div>					
<div><div><div><div><div>ASUS®</div><div>Title :</div></div><div><div>Engineer: <i>Peter Lo</i></div><div><div><div>Size</div><div>Project Name</div><div>Rev</div></div><div><div><i>A</i></div><div><i>Rocky30</i></div><div><i>1.0</i></div></div></div><div><div>Date: <i>Thursday, October 18, 2007</i></div><div>Sheet <i>79</i> of <i>94</i></div></div></div></div></div></div>					
	5	4	3	2	1

3.3V level logic level: DPRSLPVR, SHDN#
1.05V level logic: VID, PSI#, DPRSTP#
$$POUT = (VCSN2 - VGNDs) \times (CSP1 - CNS1 + CSP2 - CSN2) / 16.67mV$$



+5V / +3.3V POWER SUPPLY

Key Formulas:

- $V_{out} = 1V * (1 + R_c / R_d)$ (for 3V)
- $V_{out} = 1V * (1 + R_a / R_b)$ (for 5V)

Key Components:

- TPS51120RHBR (U8100A)
- MIC5235YM5 (U8101)
- Q8101, Q8102, Q8103, Q8105B, Q8105A (Transistors)
- R8101, R8102, R8103, R8104, R8105, R8106, R8107, R8108, R8109, R8110, R8111, R8112, R8113, R8114, R8115 (Resistors)
- C8101, C8102, C8103, C8104, C8105, C8106, C8107, C8108, C8109, C8110, C8111, C8112, C8113, C8114, C8115, C8116, C8117 (Capacitors)
- L8101, L8102 (Inductors)

Output Specifications:

- +3VSUS (4.568A)
- +5VSUS (5.061A)
- +3V (0.055A)
- +5V (0.04A)
- +12VSUS (0.1A)

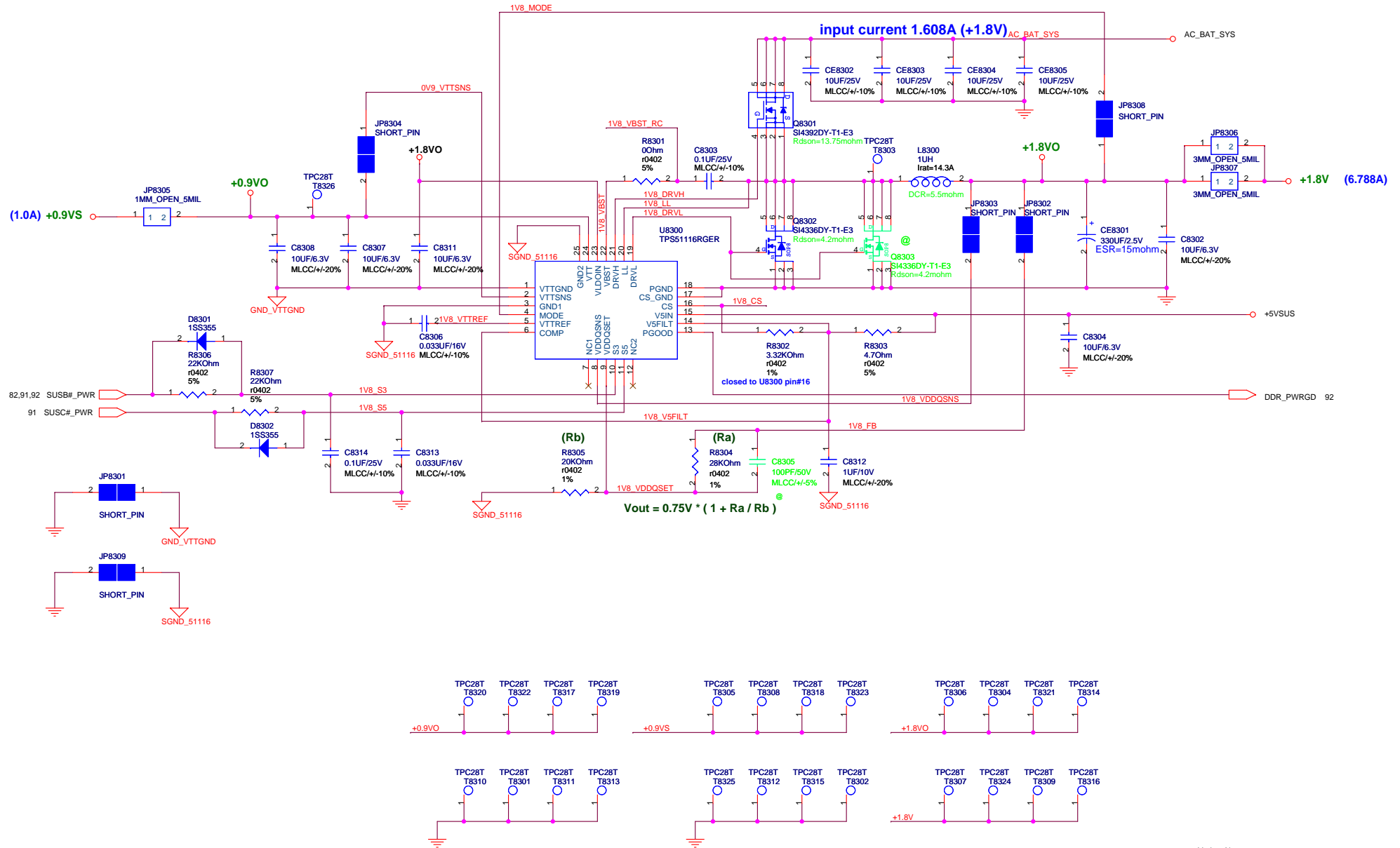
ASUS Logo and Project Information:

ASUS
Title: POWER_SYSTEM
Engineer: Kevin Chang
Project Name: Rocky 30
Date: Monday, February 04, 2008
Sheet: 81 of 94

(TONSEL = FLOAT, 1.5V = 360KHz /
1.05V = 300KHz)




+1.8V / +0.9VS POWER SUPPLY



<Variant Name>

ASUS		Title : POWER_IO_DDR & VTT	
<OrgName>		Engineer: Kevin Chang	
Size	Project Name	Rev	
Custom		Rocky 30	
Date: Monday, February 04, 2008	Sheet	83	of 94


	5	4	3	2	1
D					
C					
B					
A					


		Title : PWR_-****	
Engineer:			
<OrgName>			
Size	Project Name		Rev
A4	Rocky30		1.0
Date: Saturday, January 26, 2008		Sheet	84 of 94



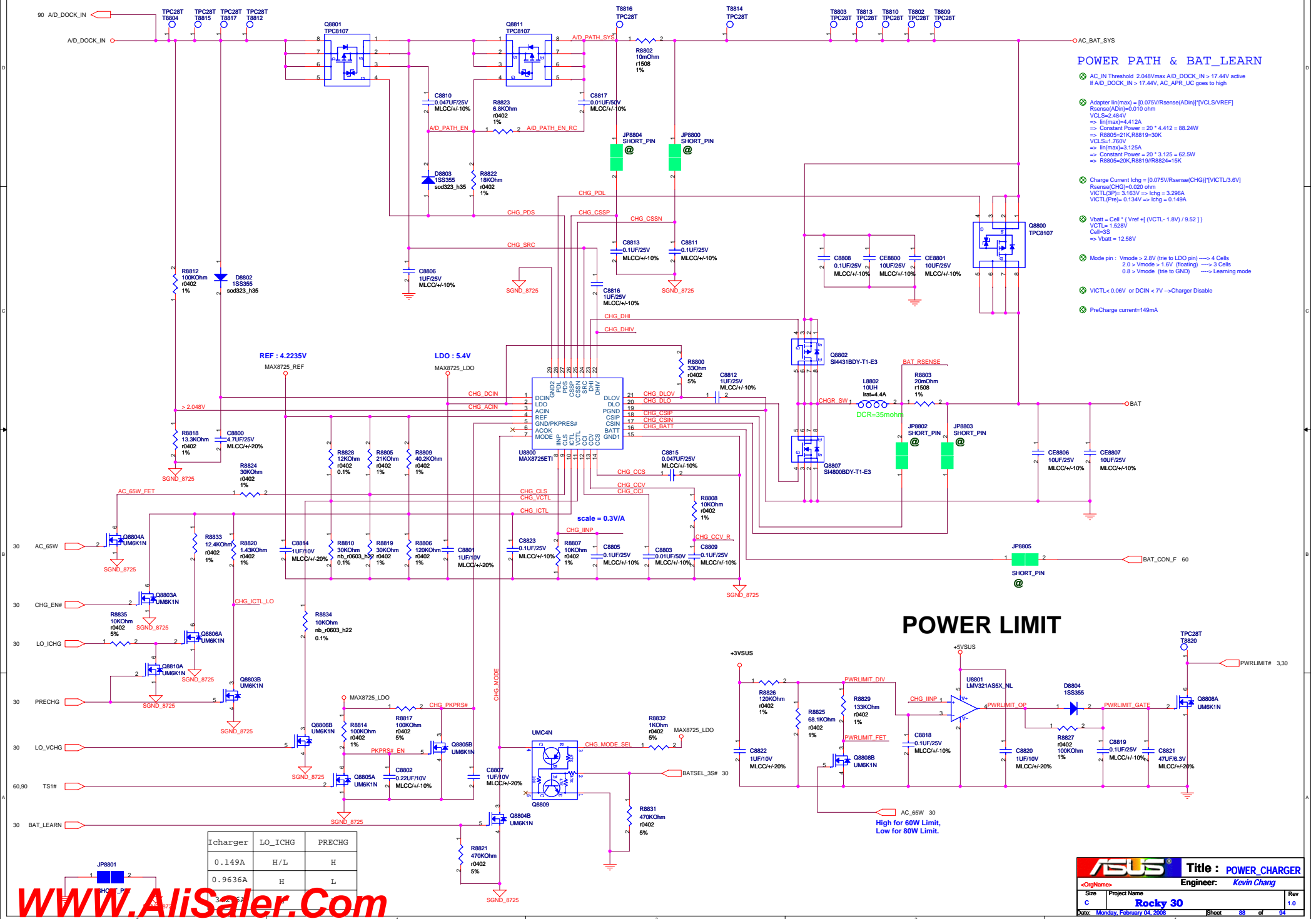
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		Title :	
<OrigName>		Engineer: <i>Kevin Chang</i>	
Size	Project Name		Rev
Custom	Rocky30		1.0
Date: <i>Friday, January 11, 2008</i>	Sheet	85	of 94

		Title : PWR_-****	
<OrgName>		Engineer: Kevin Chang	
Size A4	Project Name Rocky30		Rev 1.0
Date: Friday, January 11, 2008		Sheet	86 of 94


		Title : POWER_SHUTDOWN#	
Engineer:			
Size	Project Name		Rev
A4	Rocky30		1.0
Date: Saturday, January 26, 2008		Sheet	87 of 94

BATTERY CHARGER

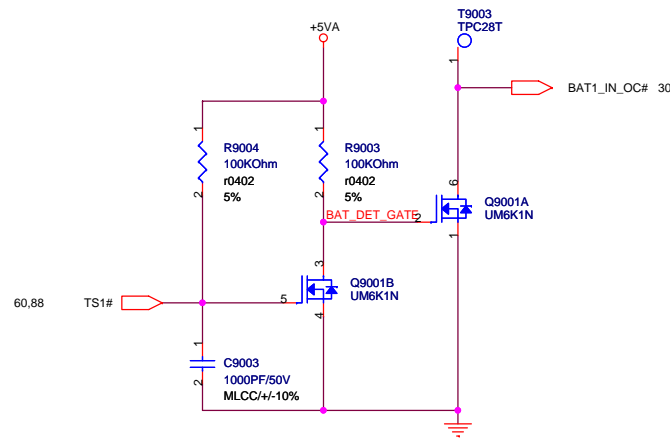


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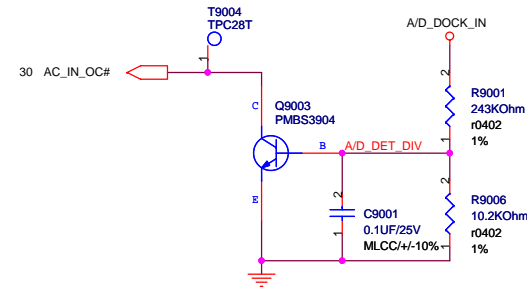
5	4	3	2	1
D				
C				
B				
A				

		Title : TFT-LCD DRIVE	
<OrgName>		Engineer:	
Size	Project Name		Rev
A4	Rocky30		1.0
Date:	Friday, January 11, 2008		Sheet 89 of 94

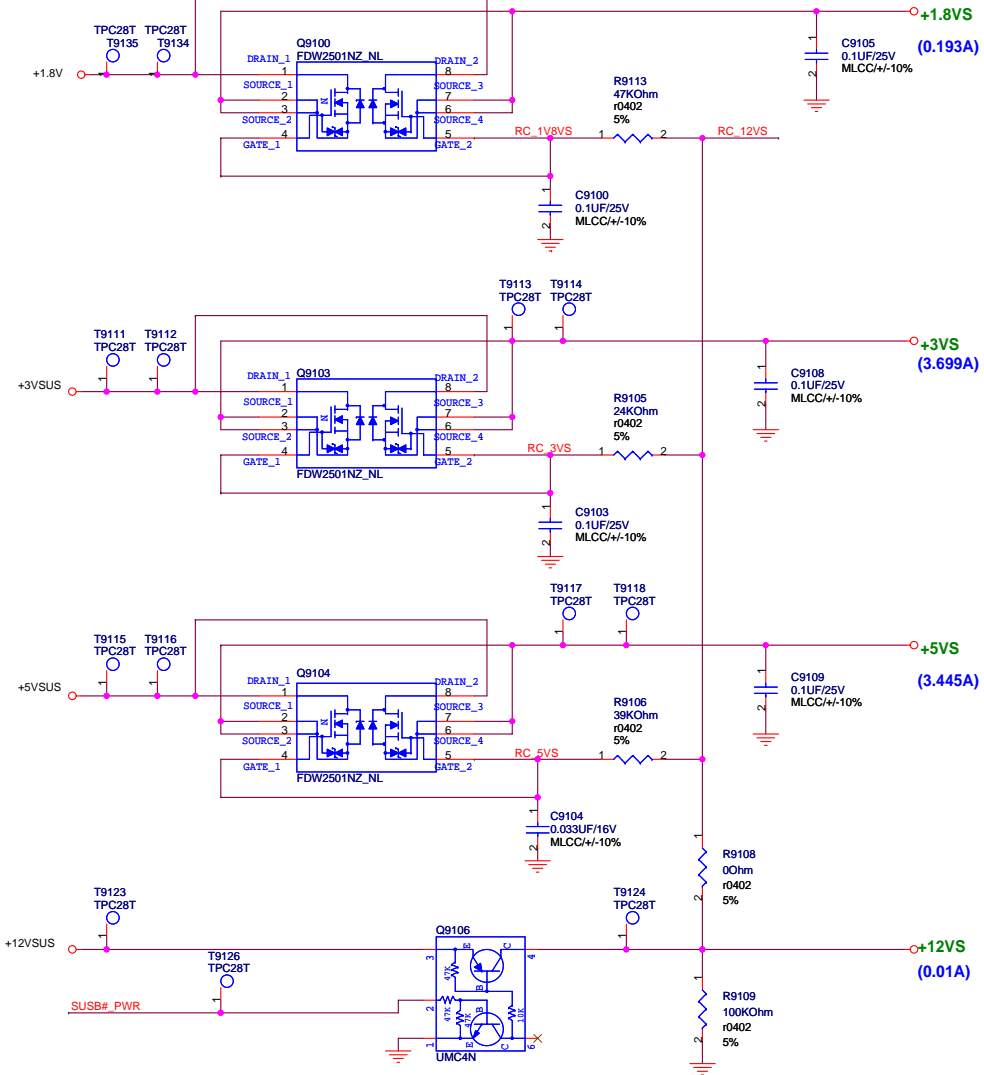
BATTERY IN DETECT



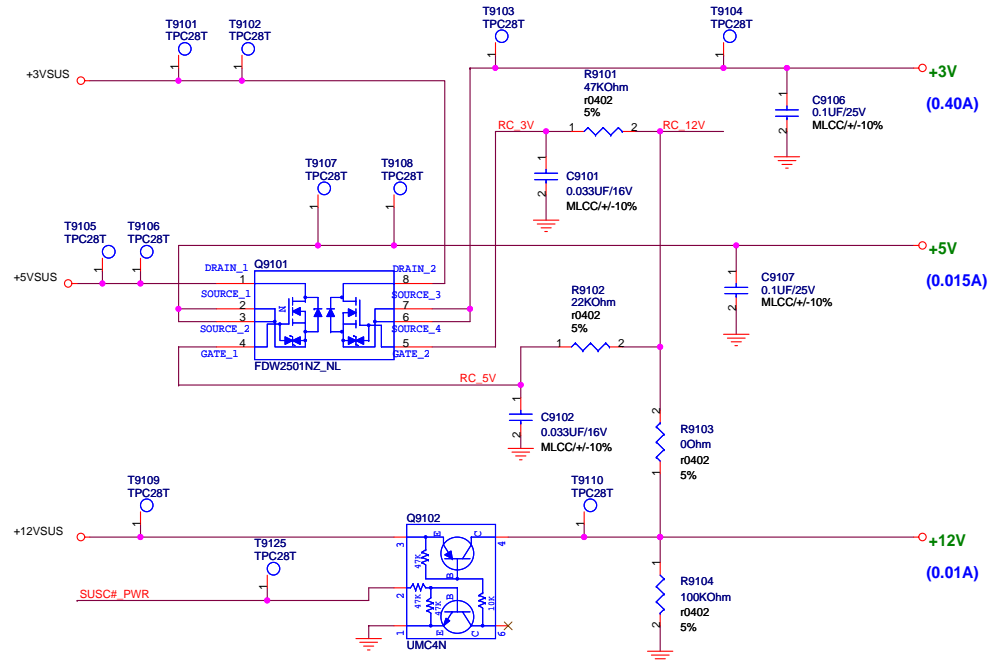
ADAPTER IN DETECT



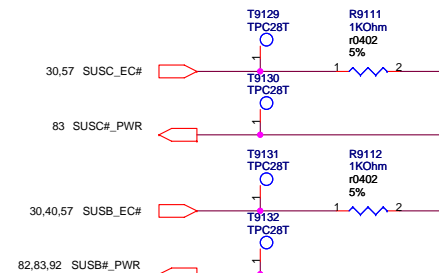
SUSB#_PWR Load SW



SUSC#_PWR Load SW



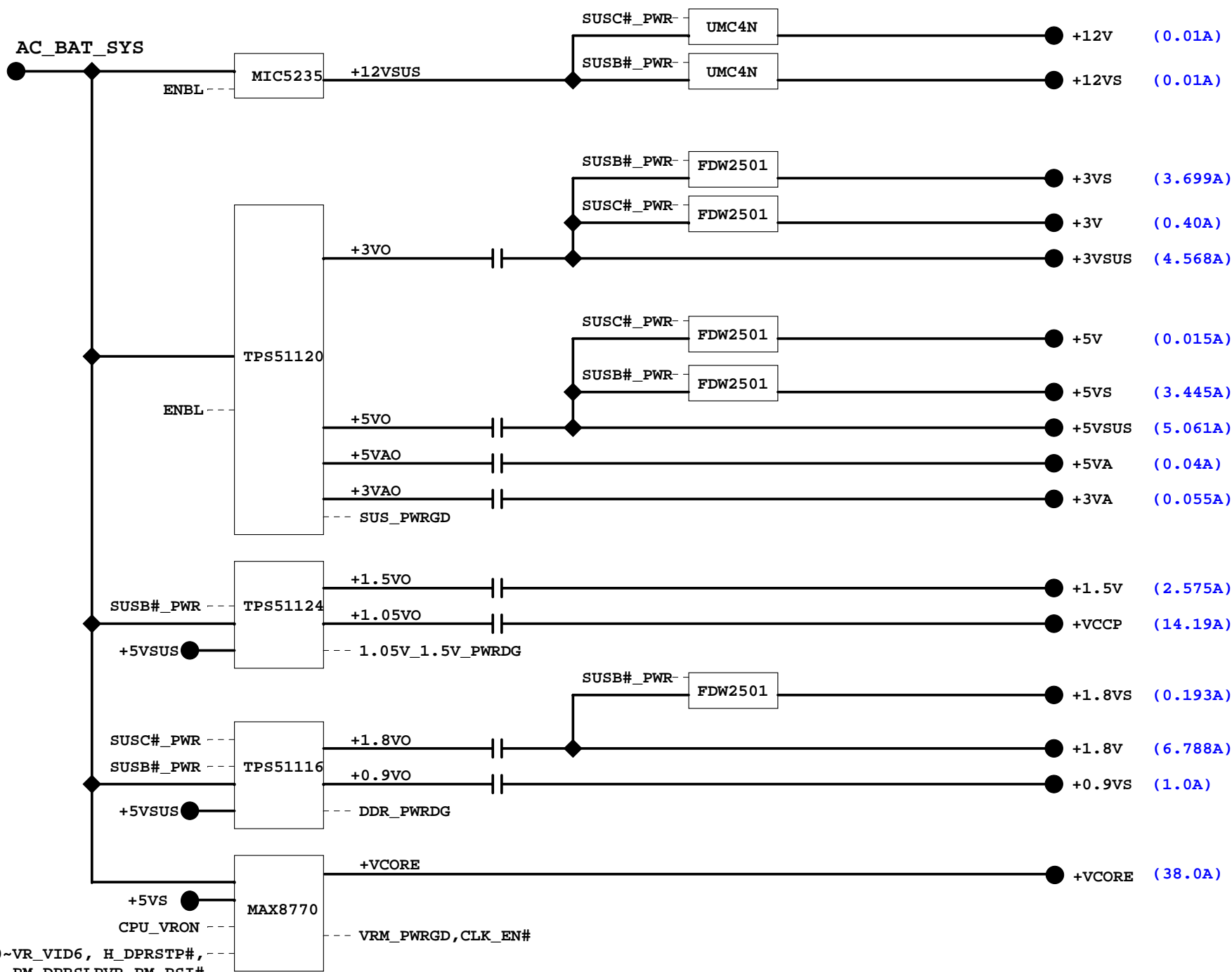
Enable Signal



POWER GOOD DETECTER







VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#